
Contents

Quotation	ix
Preface	xi
Introduction	xv
Chapter 1. Coding and Addressing Modes	1
1.1. Encoding and formatting an instruction	1
1.1.1. Code compression	8
1.2. Addressing modes	8
1.2.1. Immediate addressing.	10
1.2.2. Register addressing	11
1.2.3. Memory addressing modes.	12
1.2.4. Other addressing modes	24
1.2.5. Summary on addressing	31
1.3. Conclusion	32
Chapter 2. Instruction Set and Class	33
2.1. Definitions	33
2.2. Transfer instructions.	35
2.2.1. Data transfer.	35
2.2.2. Address manipulation instructions	37
2.3. Data processing instructions	37
2.3.1. Arithmetic instructions for integers	37
2.3.2. Bit manipulation instructions	38
2.4. Control transfer instructions	49
2.4.1. Branchings.	50
2.4.2. Conditional execution	56

2.4.3. Iteration control	59
2.4.4. Subroutine call and return instructions	62
2.5. Environmental instructions	63
2.5.1. Interrupt request and interrupt return instructions	63
2.5.2. Stopping instructions	63
2.5.3. Processor management	64
2.5.4. Memory management.	64
2.5.5. Hardware detection	65
2.5.6. Debugging	66
2.5.7. Updating	66
2.5.8. Verification	66
2.5.9. Various.	66
2.6. Parallelism instructions	66
2.6.1. Atomic instructions	66
2.6.2. Synchronization instructions	68
2.7. Extensions to instruction sets	68
2.7.1. Multimedia extension.	68
2.7.2. Extension for signal processing	71
2.7.3. Cryptography	72
2.7.4. Randomization management.	72
2.7.5. Implications	72
2.8. Various instructions	72
2.8.1. Instructions for handling (strings of) characters	72
2.8.2. Input/output instructions	73
2.8.3. High-level instructions	73
2.8.4. Arithmetic instructions specific to a representation of particular numbers.	73
2.8.5. An unusual instruction	75
2.9. Conclusion	75
Chapter 3. Additional Concepts.	77
3.1. Concepts associated with the instruction set and programming	77
3.1.1. Illegal, non-implemented, invalid, reserved and trusted instructions	77
3.1.2. Alignment or framing of instructions	78
3.1.3. Orthogonality and symmetry.	80
3.1.4. Pure, re-entrant and relocatable codes and code for read-only memory	81
3.1.5. Levels of programming languages.	82
3.2. Concepts linked to execution	83
3.2.1. Consequences for execution time and memory requirements	83
3.2.2. Execution modes	84
3.2.3. Portability	88
3.2.4. Virtualization	88
3.3. Hardware and software compatibilities	90

3.3.1. Hardware compatibility	90
3.3.2. Software compatibility	90
3.3.3. Upward and downward compatibilities	91
3.4. Measuring processor performances	93
3.4.1. Clock rate	94
3.4.2. Number of instructions per cycle	95
3.4.3. Execution time	97
3.4.4. Benchmark suites	97
3.4.5. Development of performances over time	101
3.5. Criteria for choosing.	102
3.6. Conclusion	103
Chapter 4. Subroutine	105
4.1. Stack memory	105
4.2. Subroutine	113
4.2.1. Nested calls	115
4.2.2. Execution context.	116
4.2.3. Passing parameters and call conventions	116
4.3. Conclusion	118
Chapter 5. Interrupt Mechanism	119
5.1. Origin, definition and classification	119
5.2. External causes.	121
5.2.1. Execution context.	125
5.2.2. Sources.	125
5.2.3. Masking	127
5.2.4. Consideration and priority	129
5.2.5. Interrupt controller	132
5.3. Nested interrupts.	133
5.4. Internal causes	135
5.5. Debugging	138
5.6. Priority between internal and external interrupts	139
5.7. Identification of the source and vectorization	146
5.8. Nested and queued interrupts	152
5.9. Uses.	153
5.10. Interrupts and execution modes	154
5.11. Interrupts and advanced architectures	155
5.12. Conclusion	162

Conclusion of Volume 4	163
Exercises	165
Appendix	171
Acronyms	177
References	197
Index	211