
Contents

Preface	ix
Introduction	xiii
Chapter 1. Discrete-time Signals and Systems	1
1.1. Discrete-time signals	1
1.1.1. “Dirac comb” and series of samples	1
1.1.2. Sampling (or Shannon’s) theorem, anti-aliasing filtering and restitution of the continuous-time signal using the Shannon interpolation formula	8
1.1.3. Discrete Fourier series (or transform); “fast Fourier transform” (FFT) and discrete cosine transforms (DCT)	11
1.2. Discrete time–continuous time interface circuits	14
1.2.1. Real sampler	14
1.2.2. Sample-and-hold circuit	17
1.2.3. Interpolation circuits and smoothing methods for sampled signals	20
1.3. Phase-shift measurements; phase and frequency control; frequency synthesis	24
1.3.1. Three-state circuit for measuring the phase shift	24
1.3.2. Phase-locked loop	30
1.3.3. Phase and frequency modulator and demodulator; locking and dynamic operation of the loop	33
1.3.4. Analog frequency synthesis	39
1.3.5. Digital synthesis and phase and frequency control systems	45
1.4. Sampled systems	55
1.4.1. Z-transform for systems described by a recurrence equation (or difference equation)	55
1.4.2. Continuous-time systems subject to a sampled signal	61

1.4.3. Switched-capacitor circuits and infinite impulse response (IIR) filters	63
1.4.4. Switched-capacitor circuits adapted to finite impulse response (FIR) filters	72
1.4.5. Sampled systems modeling using functional blocks	74
1.4.6. Synthesis of sampled filters	76
1.4.7. Filtering and digital processing	91
1.5. Discrete-time state-space form	99
1.6. Exercises	104
1.6.1. Switched-capacitor first-order high-pass filter	104
1.6.2. Basic switched-capacitor-based filter operator (IIR) using an ideal operational amplifier.	107
1.6.3. Delay operator with offset correction and FIR filtering	113
1.6.4. Phase-locked loops	117
1.6.5. Sampled models of the PLL.	124
1.6.6. Discrete-time systems in state-space form	127
Chapter 2. Quantized Level Systems: Digital-to-Analog and Analog-to-Digital Conversions	137
2.1. Quantization noise.	137
2.2. Characteristics of converters.	140
2.2.1. Dynamics and resolution	140
2.2.2. Static errors	140
2.2.3. Dynamic operation	142
2.3. Digital-to-analog conversion.	143
2.3.1. Current- or voltage-weighted systems of 2^n dynamics in binary code	143
2.3.2. Iterative resistance of a network of voltage and current dividers	144
2.3.3. R-2R ladders	145
2.3.4. Charge redistribution capacitive converters.	147
2.4. Analog-to-digital conversion	154
2.4.1. Converter using 2^n comparators or flash converter	154
2.4.2. Converters based on n successive approximations	156
2.4.3. Mixed or semi-flash converter	159
2.4.4. Ramp converters	160
2.5. "Sigma-delta" conversions.	161
2.5.1. Basic first-order modulator-based "sigma-delta" ADC.	162
2.5.2. First-order modulator sampled model	166
2.5.3. Modulators of order $l > 1$ and signal-to-noise ratio	167
2.5.4. Stable modulators of order greater than two and CMOS technology-based circuitry	172

2.5.5. Decimation filter	177
2.5.6. “Sigma-delta” DAC	182
2.6. Exercises	186
2.6.1. DAC based on R-2R network and current sources	186
2.6.2. Series DACs based on redistribution of charge	188
2.6.3. Parallel DACs based on redistribution of charge and reduced capacitance.	195
2.6.4. Basic “delta-sigma” ADC.	197
2.6.5. Third-order “MASH” modulator.	199
2.6.6. Third-order digital filter of a multi-bit “sigma-delta” DAC	201
Bibliography	209
Index	211