

*Series Editor*  
*Robert Baptist*

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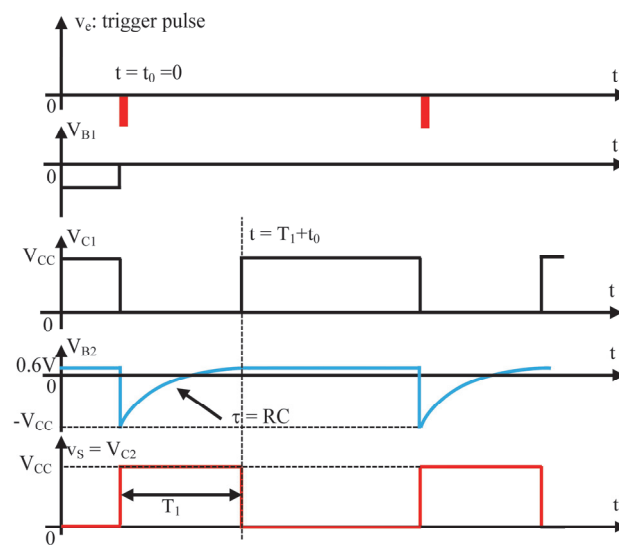
# **Nonlinear Electronics 2**

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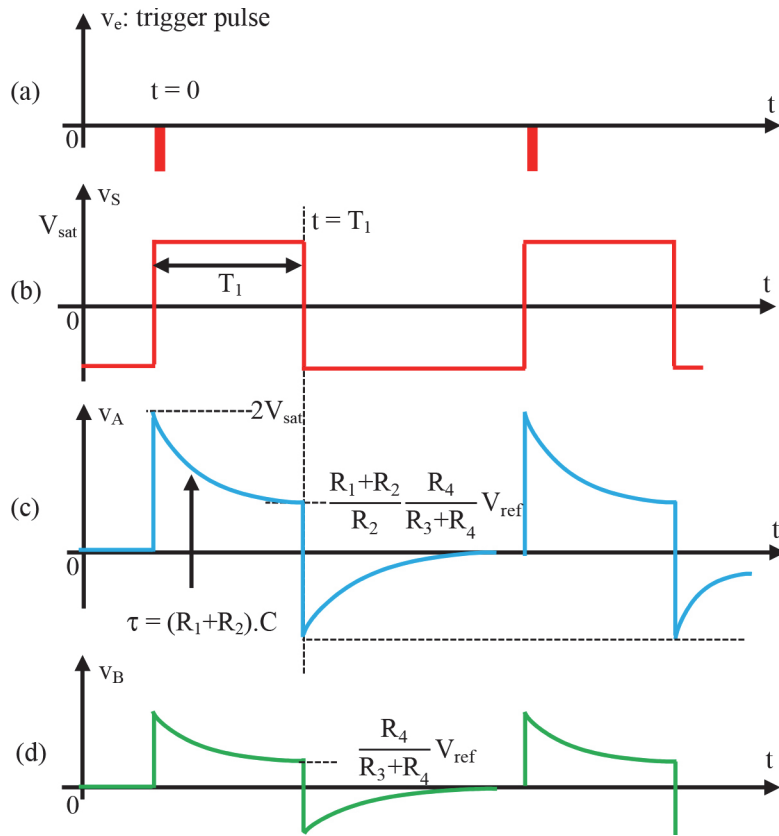
*Flip-Flops, ADC, DAC and PLL*

Brahim Haraoubia

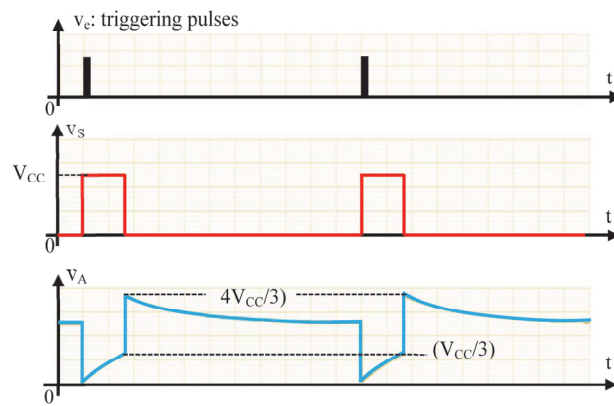
Color section



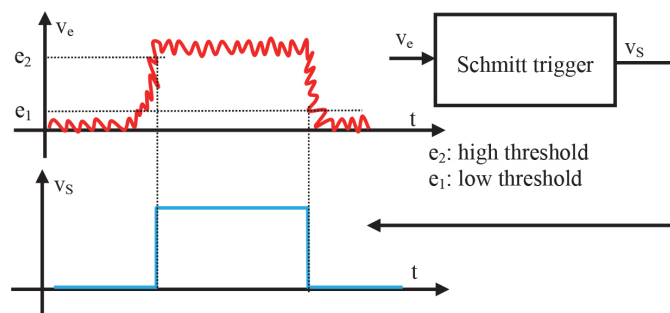
**Figure 1.6.** Signals associated with the functioning of the bipolar transistor monostable



**Figure 1.9.** Evolution of the different signals at the level of the op-amp monostable: (a) triggering signal; (b) output signal; (c) signal at point A; (d) signal at point B

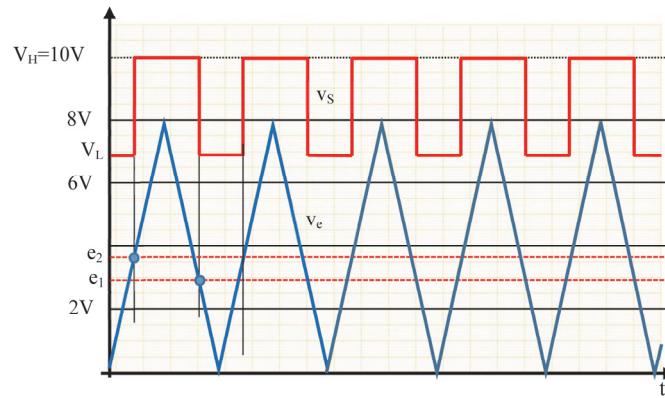


**Figure 1.13.** Signals implemented in a NOR gate monostable

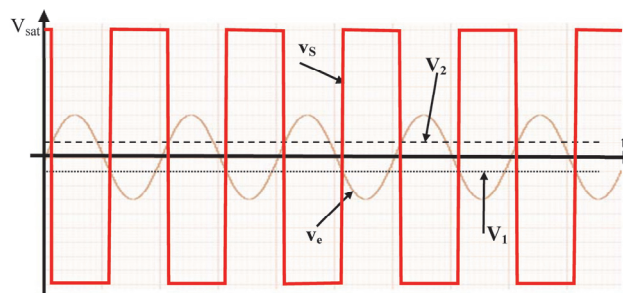


**Figure 1.26.** Application example of the Schmitt trigger: reshaping of a square wave

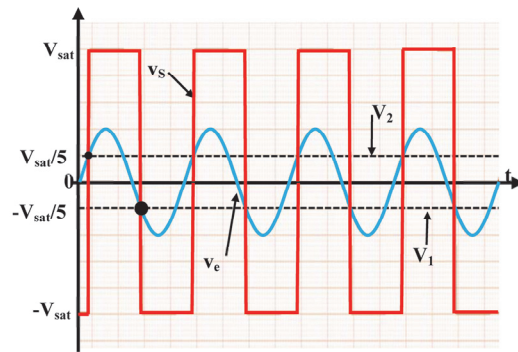




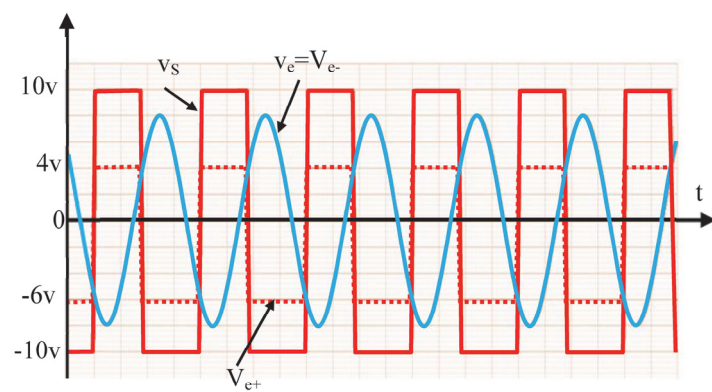
**Figure 1.31.** Variation of the output signal corresponding with the signal applied to the input of the bipolar transistor Schmitt trigger



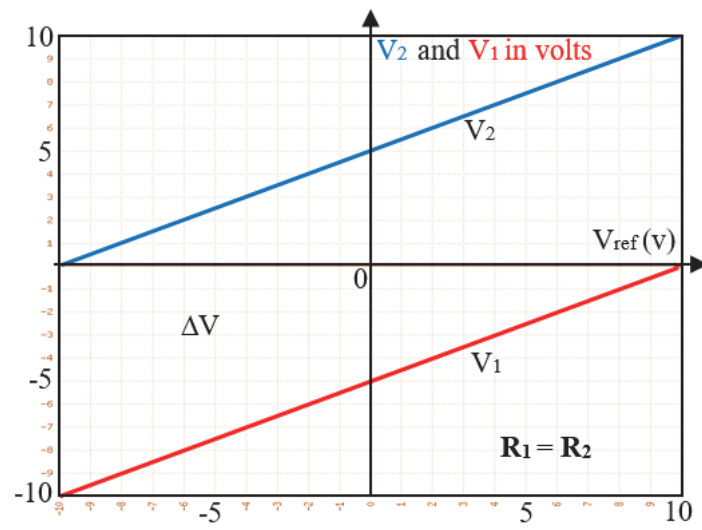
**Figure 1.33.** Evolution of the output signal  $v_s$  compared to the signal  $v_e$  applied to the input of an op-amp Schmitt trigger



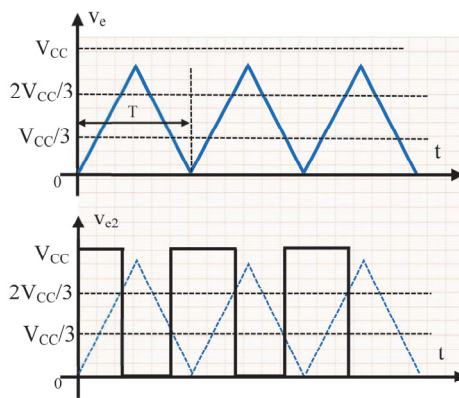
**Figure 1.36.** Signals involved at the non-inverting Schmitt trigger level



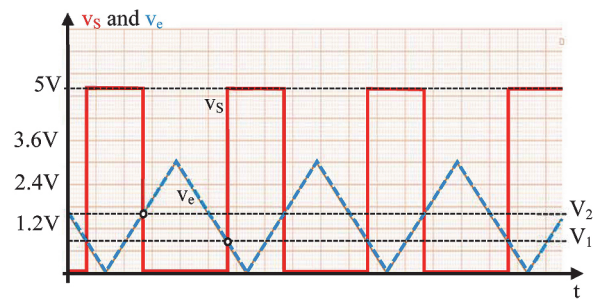
**Figure 1.39.** Signals involved in a Schmitt trigger with adjustable thresholds



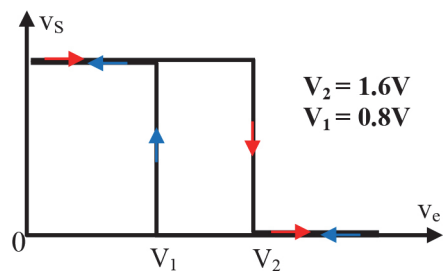
**Figure 1.40.** Evolution of switching thresholds based on the reference voltage  $V_{ref}$



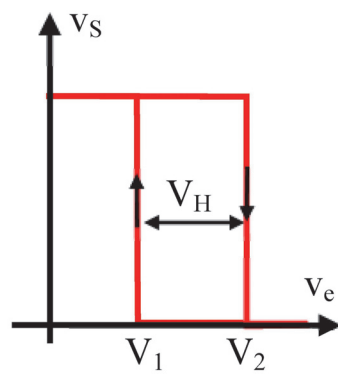
**Figure 1.42.** Evolution of the output signal according to the signal applied to the input of a Schmitt trigger designed around the 555 circuit



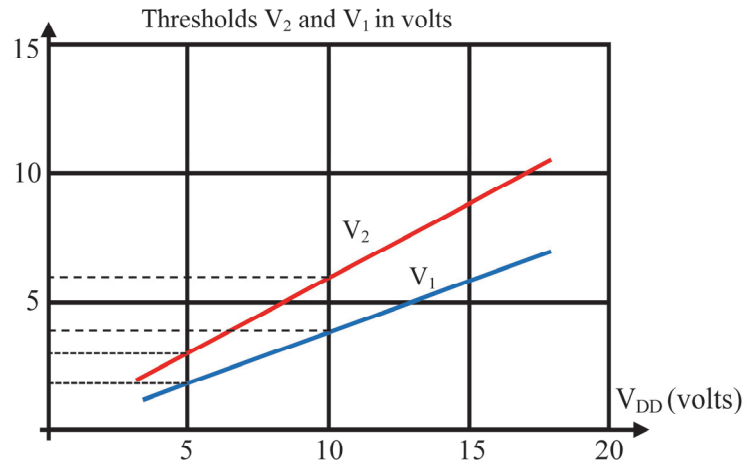
**Figure 1.46.** Evolution of the output signal according to the signal applied to the input Schmitt trigger based on the 7414 IC



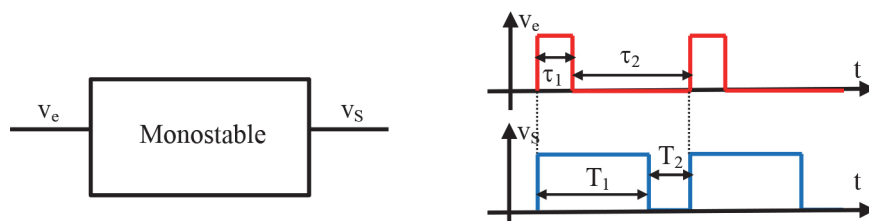
**Figure 1.47.** Hysteresis cycle of the Schmitt trigger based on the 7414 circuit



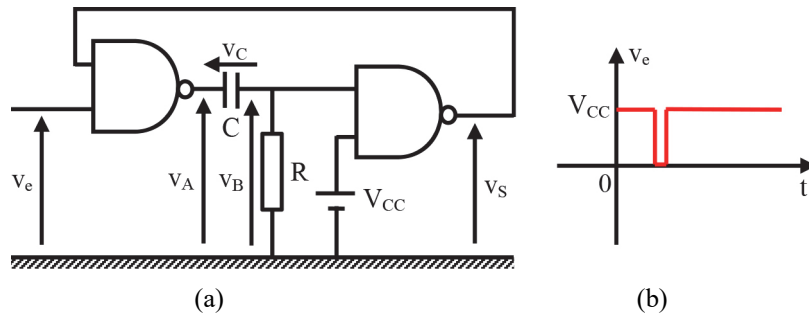
**Figure 1.50.** Hysteresis cycle of the built-in Schmitt trigger of the 4093 circuit



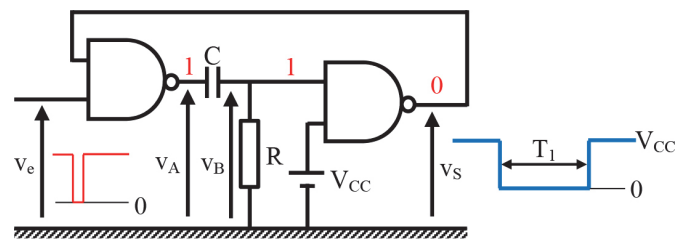
**Figure 1.51.** Evolution of the switching thresholds with the supply voltage (source: datasheet Texas Instruments)



**Figure E1.1.** (a) Monostable circuit and (b) signals involved



**Figure E2.1.** (a) Circuit under study and (b) pulse applied on input



**Figure E2.2.** Quasi-stable state of the circuit

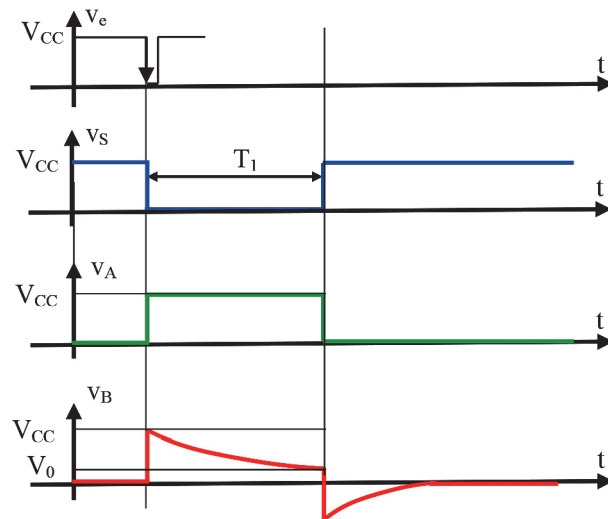


Figure E2.3. Representation over the time of voltages  $v_A$ ,  $v_B$  and  $v_s$

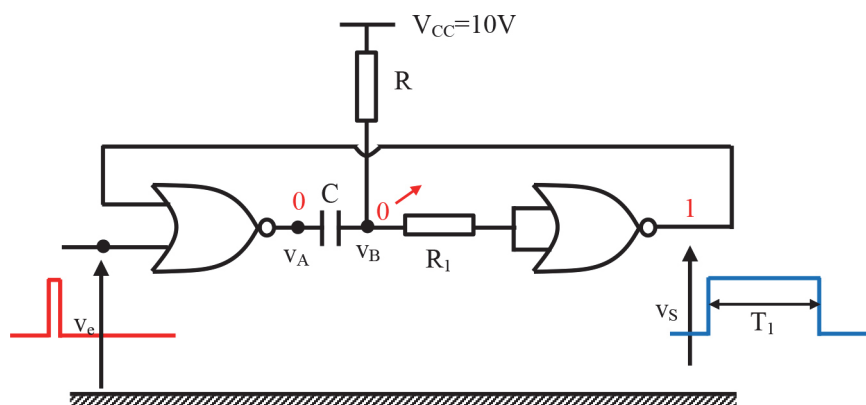
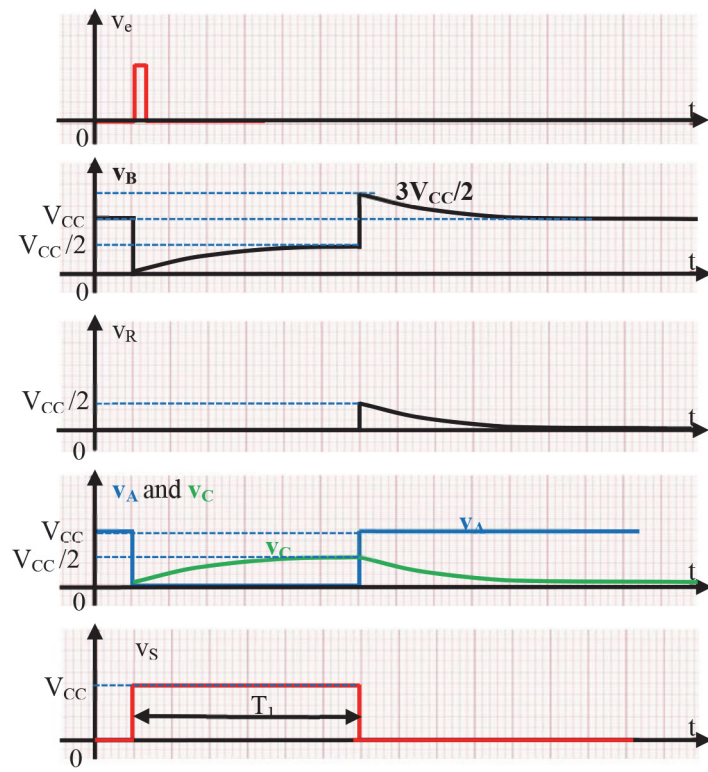
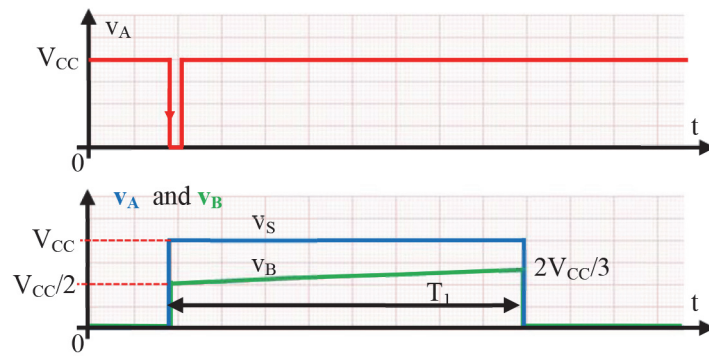


Figure E3.2. Switching of the stable state to the quasi-stable state

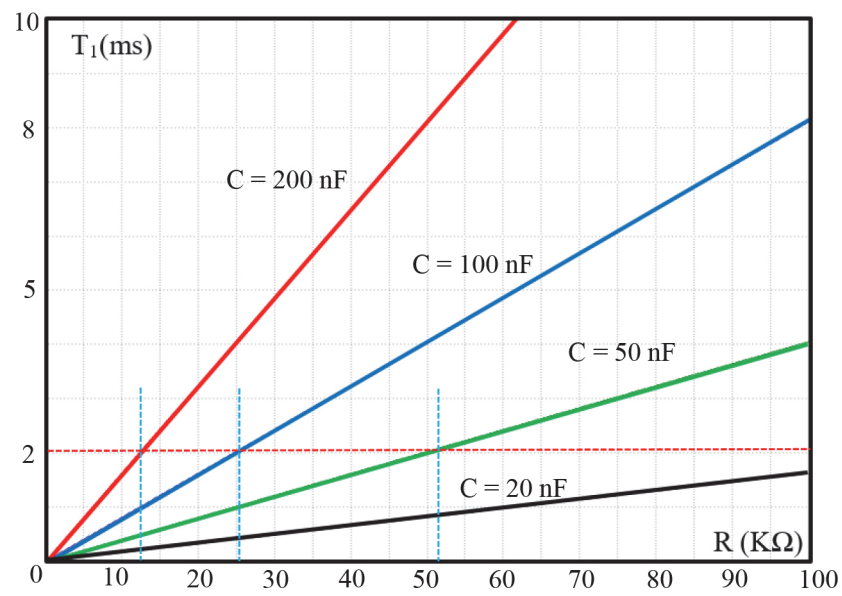


**Figure E3.3.** Representation of voltages  $v_A$ ,  $v_B$ ,  $v_R$ ,  $v_C$  and  $v_S$

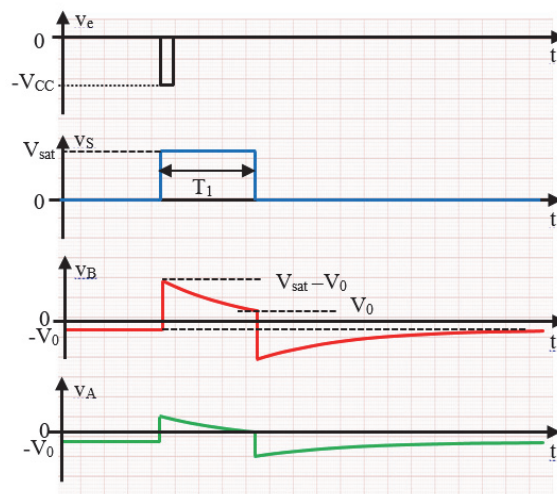




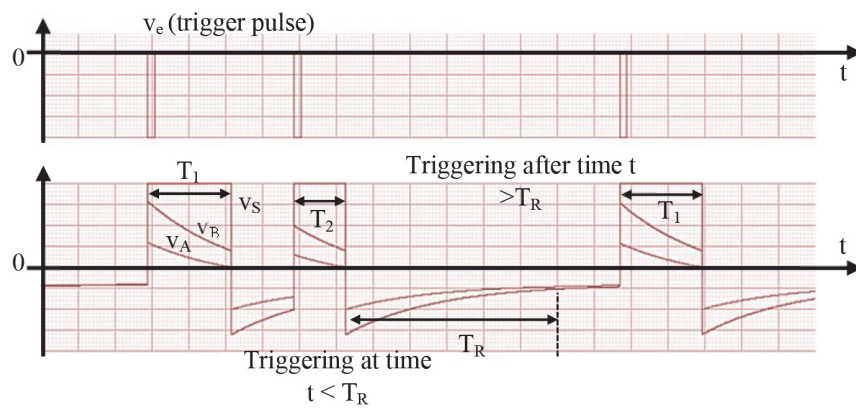
**Figure E4.2.** Evolution of voltages  $v_A$ ,  $v_B$  and  $v_S$



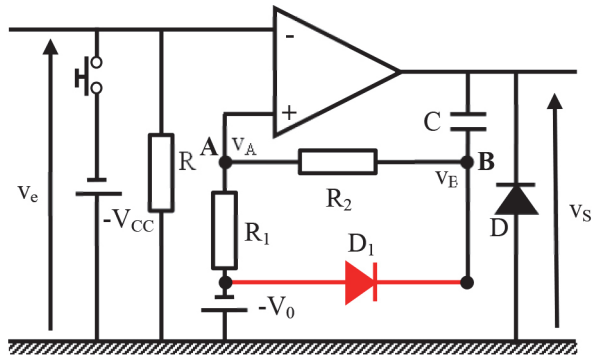
**Figure E4.3.** Evolution of the duration of the quasi-stable state according to  $R$



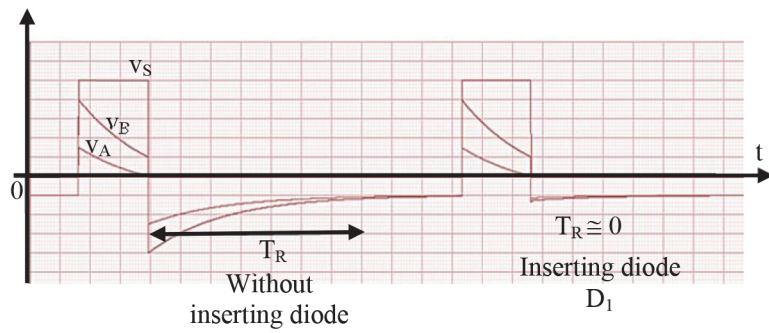
**Figure E5.3.** Evolution in time of the signals  $v_e$ ,  $v_s$ ,  $v_B$  and  $v_A$



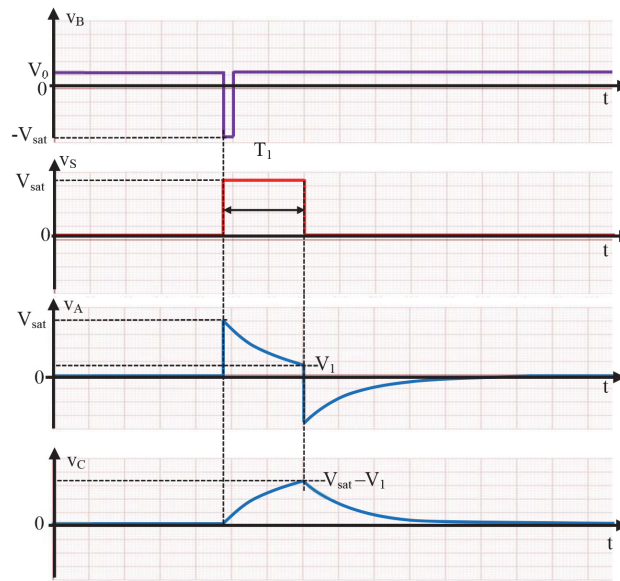
**Figure E5.4.** Effect of the recovery time on the monostable operation



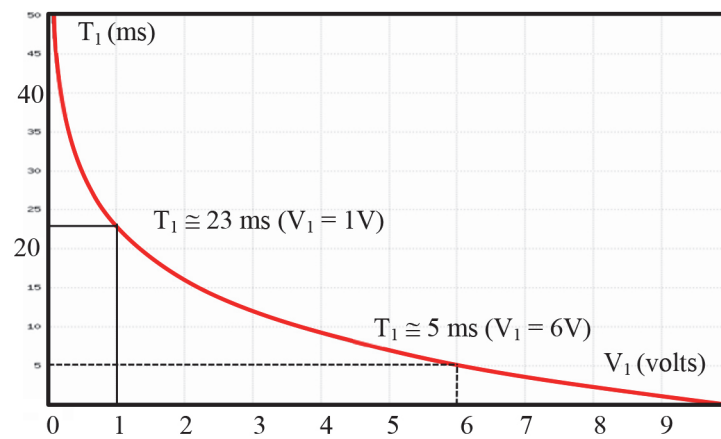
**Figure E5.5.** Insertion of diode  $D_1$  to decrease the recovery time



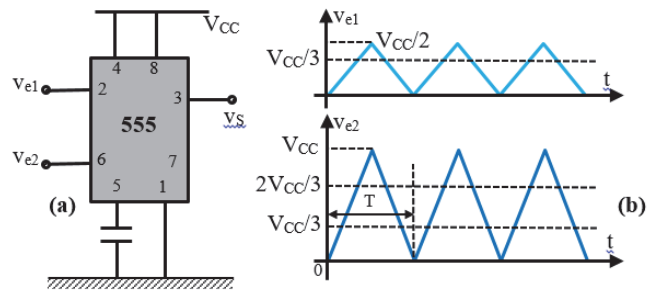
**Figure E5.6.** Effect of the diode on the recovery time



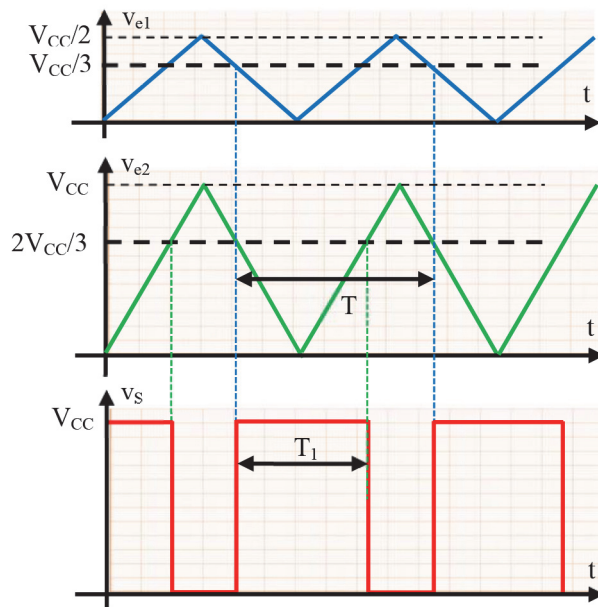
**Figure E6.2.** Representation of the evolution over time of the signals at points B, S, A and at the terminals of capacitor C for  $V_1 > 0$



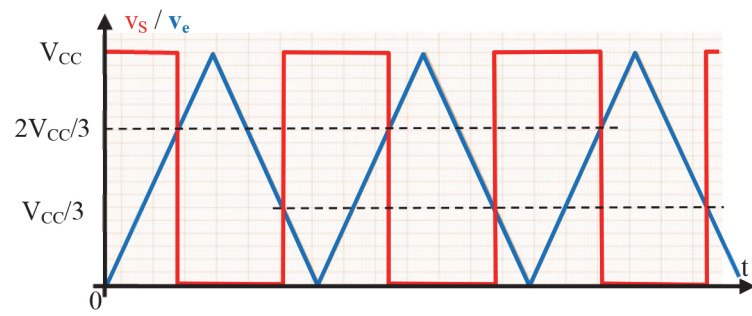
**Figure E6.3.** Evolution of the duration of the quasi-stable state according to voltage  $V_1$



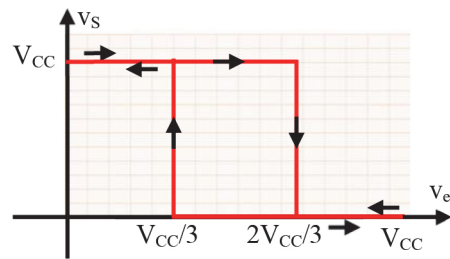
**Figure E7.1.** (a) Circuit under study and (b) signals applied on the inputs



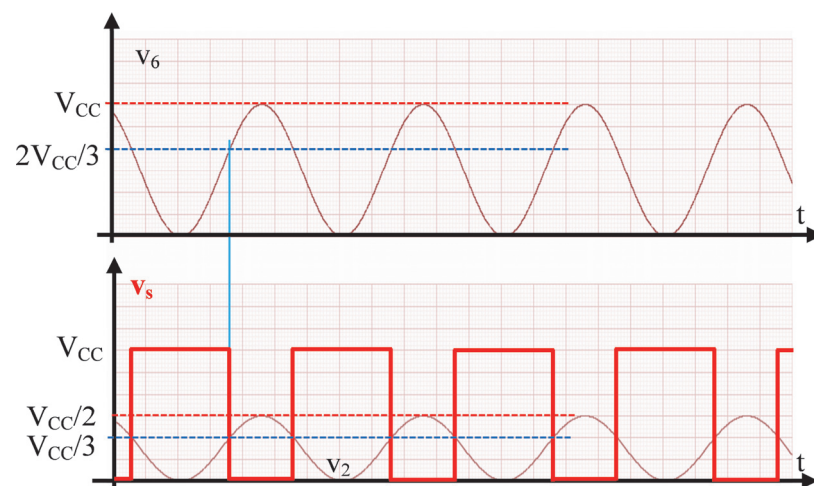
**Figure E7.3.** Representation of the evolution of the output voltage according to  $v_{e1}$  and  $v_{e2}$



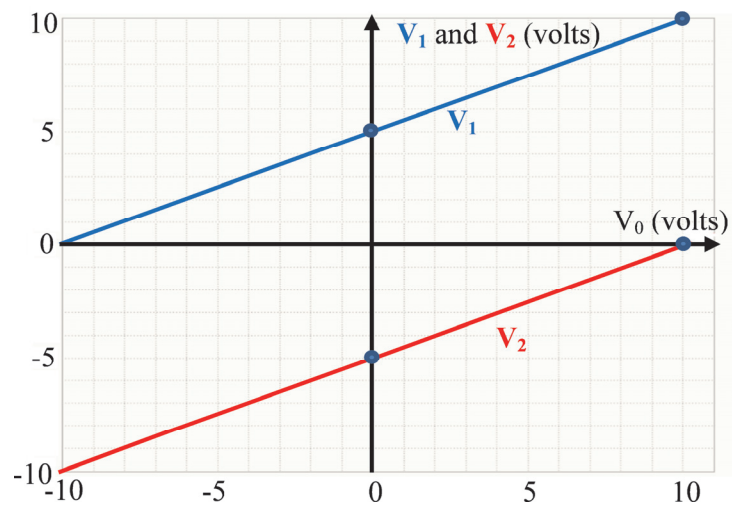
**Figure E7.4.** Evolution of the output voltage  $v_s$  according to time



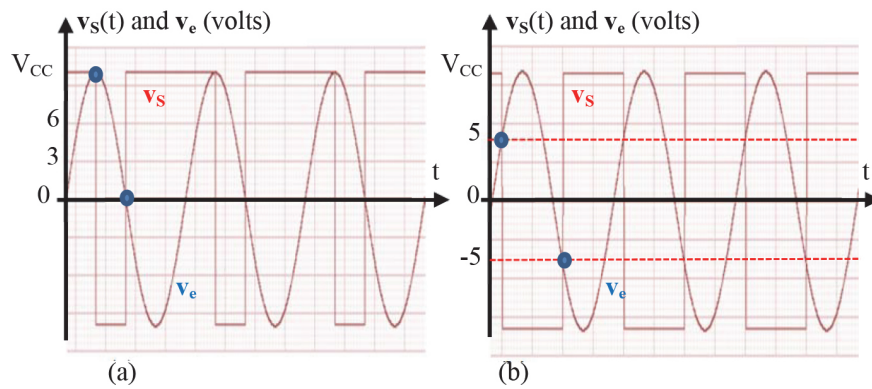
**Figure E7.5.** Evolution of the output voltage  $v_s$  according to time



**Figure E7.6.** Evolution of the output voltage vs with respect to time

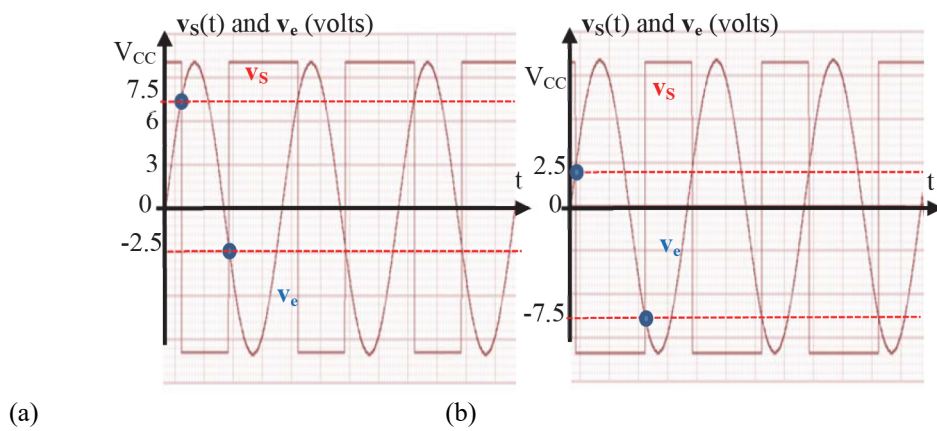


**Figure E8.2.** Evolution of the switching thresholds according to  $V_0$

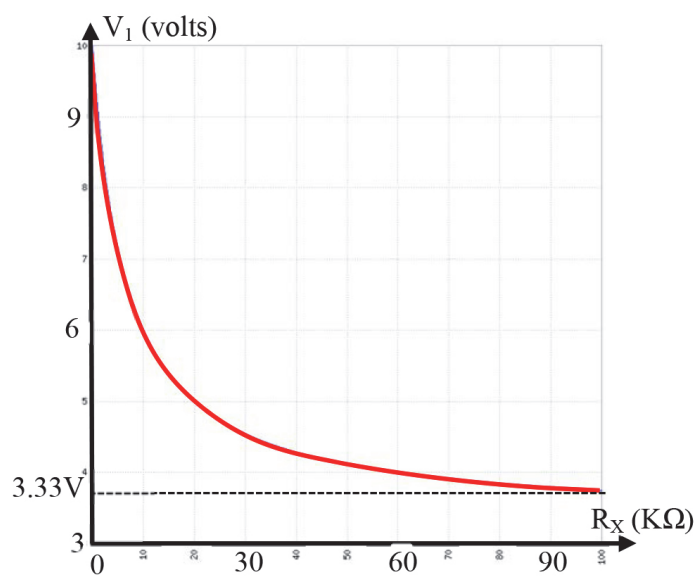


**Figure E8.3.** Representation of  $v_S(t)$ : (a)  $V_0 = V_{CC}$  and (b)  $V_0 = 0$





**Figure E8.4.** Representation of  $v_s(t)$ : (a)  $V_0 = V_{CC}/2$  and (b)  $V_0 = -V_{CC}/2$



**Figure E9.2.** Evolution of the high switching threshold according to  $R_x$

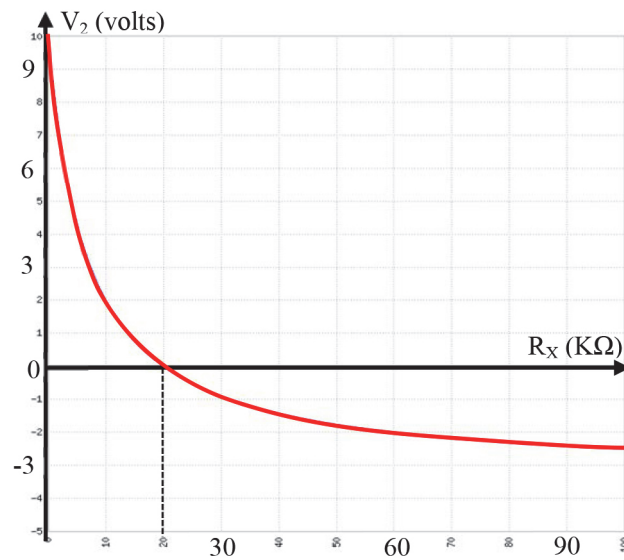


Figure E9.3. Evolution of the low switching threshold according to  $R_X$

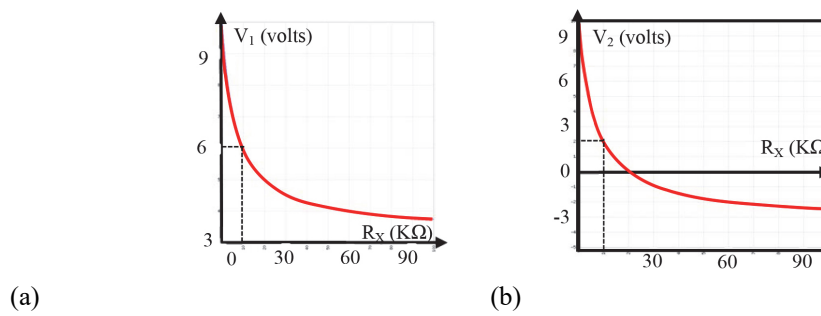
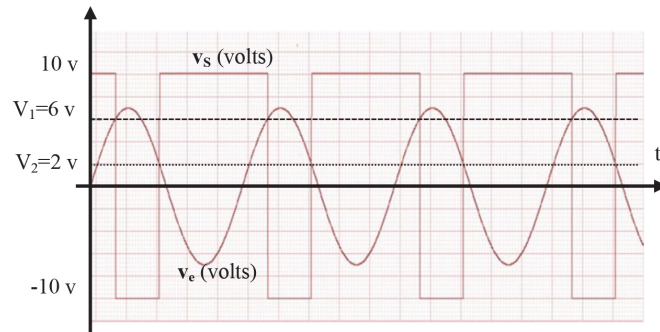
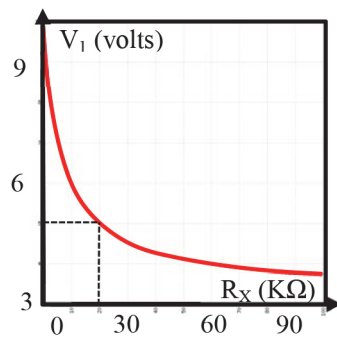


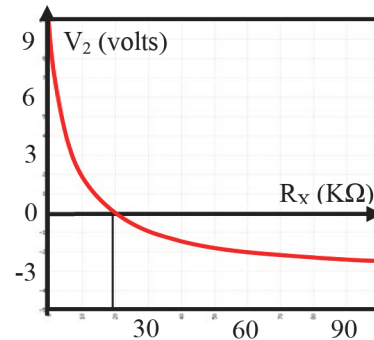
Figure E9.4. Graphical determination of the switching thresholds for  $R_X = 10 K\Omega$ : (a) high threshold and (b) low threshold



**Figure E9.5.** Evolution of the output voltage with respect to time according to the input voltage

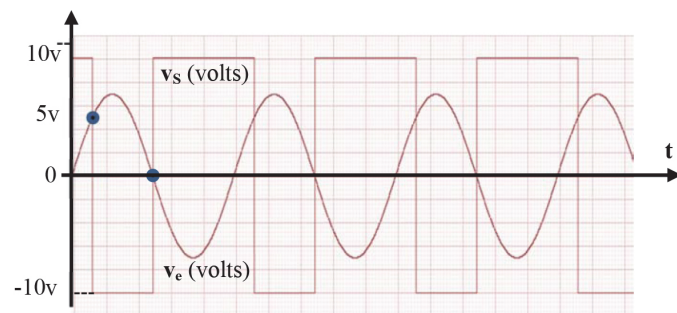


(a)

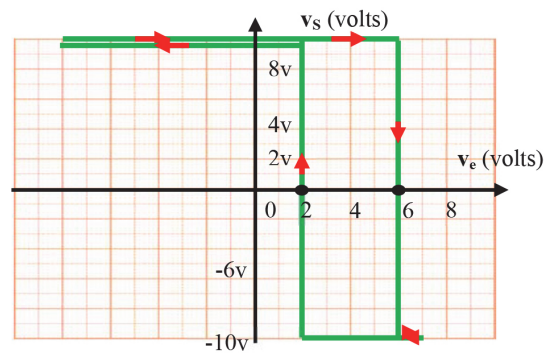


(b)

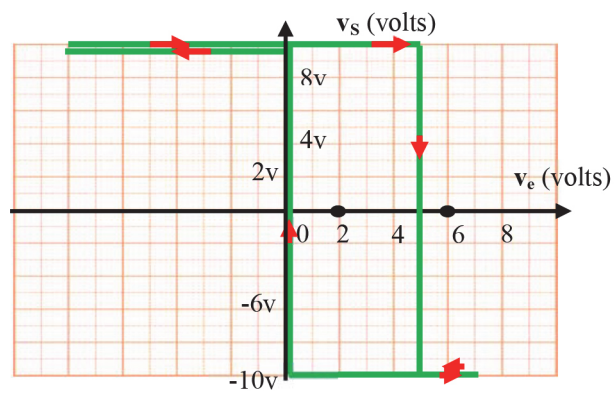
**Figure E9.6.** Graphical determination of switching thresholds for  $R_x = 20 \text{ k}\Omega$ :  
(a) high threshold and (b) low threshold



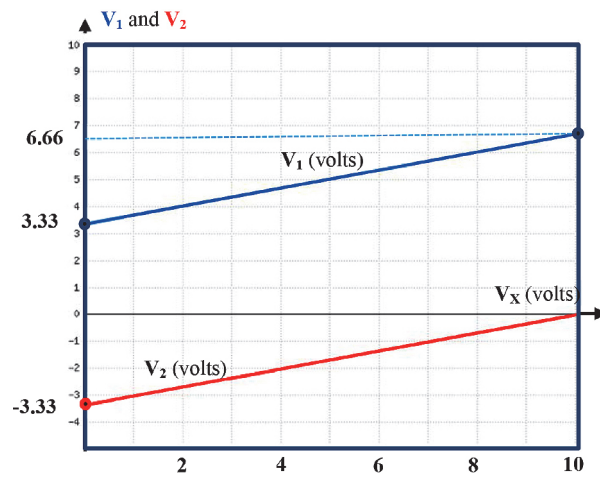
**Figure E9.7.** Evolution of the output voltage with respect to time



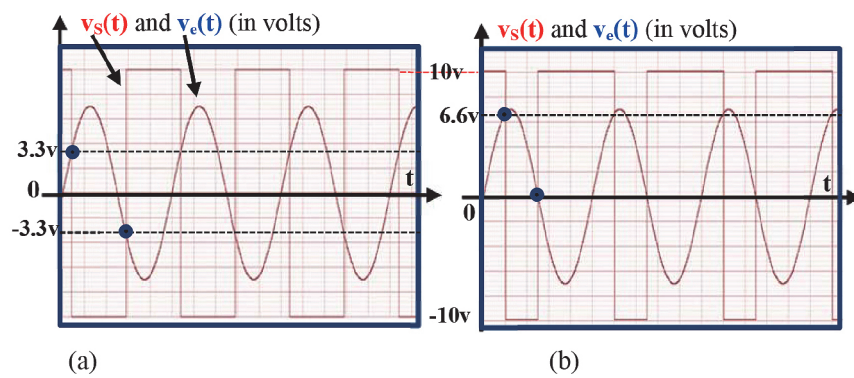
**Figure E9.8.** Evolution of  $v_s = f(v_e)$  for  $R_x = 10 \text{ k}\Omega$



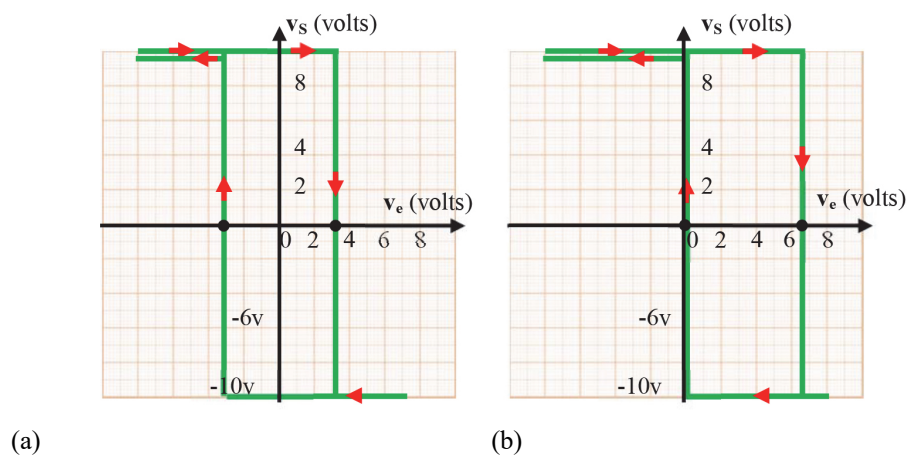
**Figure E9.9.** Evolution of  $v_s = f(v_e)$  for  $R_x = 20 \text{ k}\Omega$



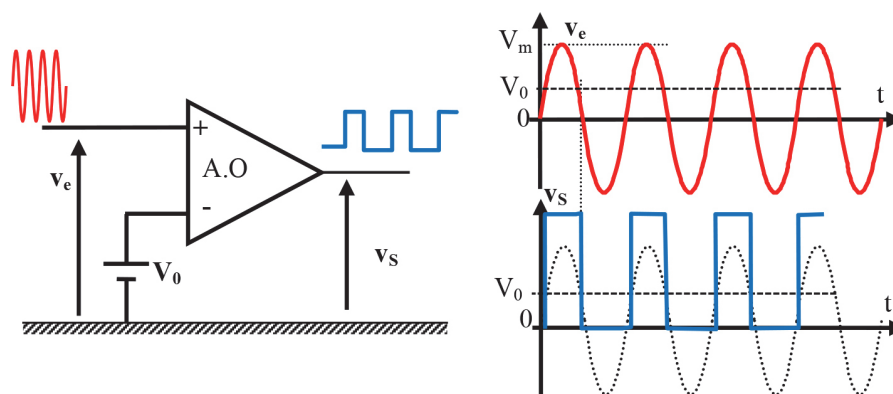
**Figure E9.10.** Evolution of the high threshold  $V_1$  and the low threshold  $V_2$  according to voltage  $V_X$



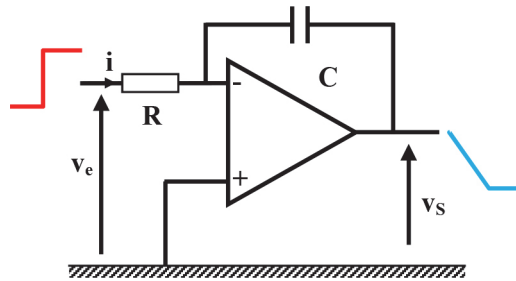
**Figure E9.11.** Plot of  $v_s(t)$ : (a)  $V_X = 0$  V and (b)  $V_X = V_{CC} = 10$  V



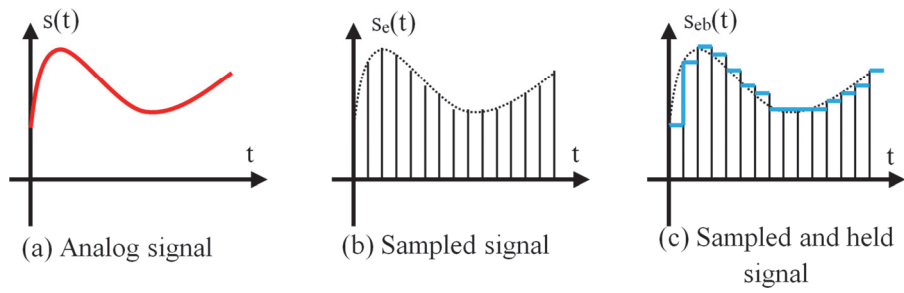
**Figure E9.12.** Plot of  $v_s = f(v_e)$ : (a)  $V_X = 0\text{ V}$  and (b)  $V_X = V_{CC} = 10\text{ V}$



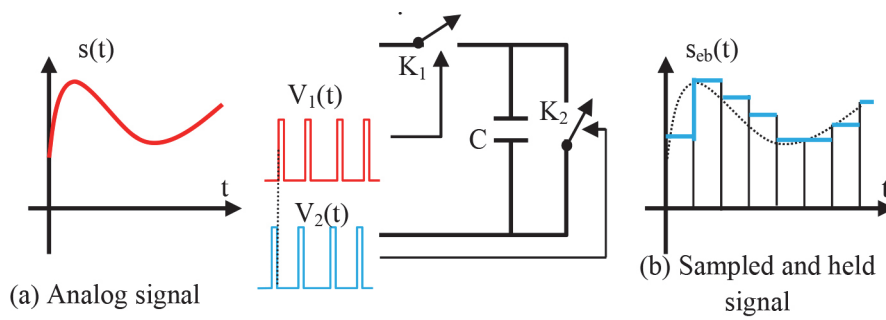
**Figure 2.5.** The output of the comparator gives at all times information about the amplitude of the input signal with respect to a reference voltage  $V_0$



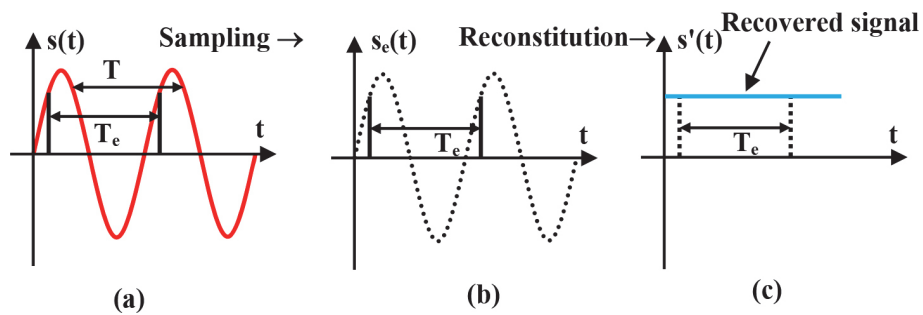
**Figure 2.6.** *Op-amp integrator circuit*



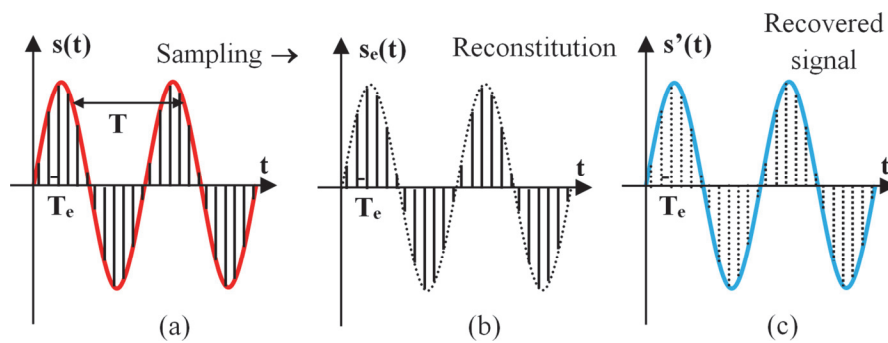
**Figure 2.12.** *Sample-and-hold principle*



**Figure 2.13.** *Basic sample-and-hold circuit*

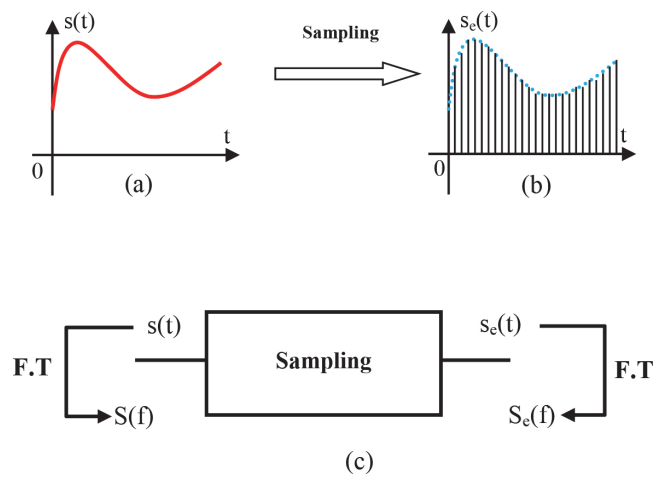


**Figure 2.14.** Sampling and reconstitution of the original signal when the sampling frequency is equal to the frequency of the original signal

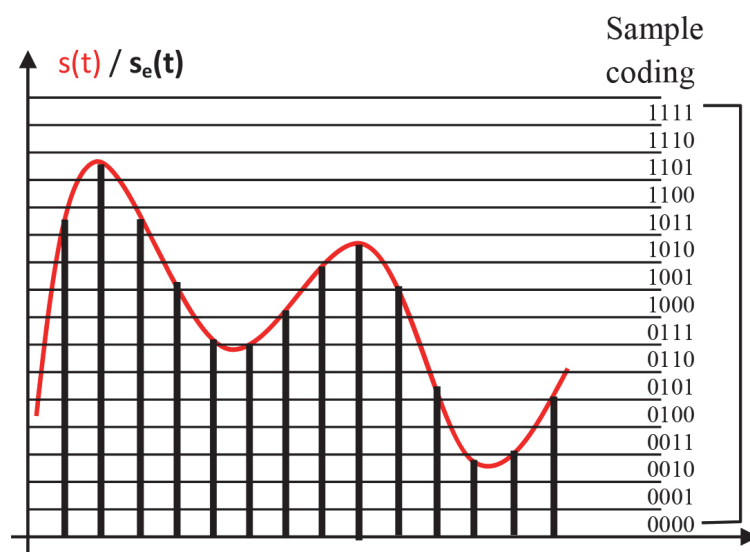


**Figure 2.15.** Sampling and reconstruction of the original signal when the sampling frequency is very large compared to the maximal frequency of the signal

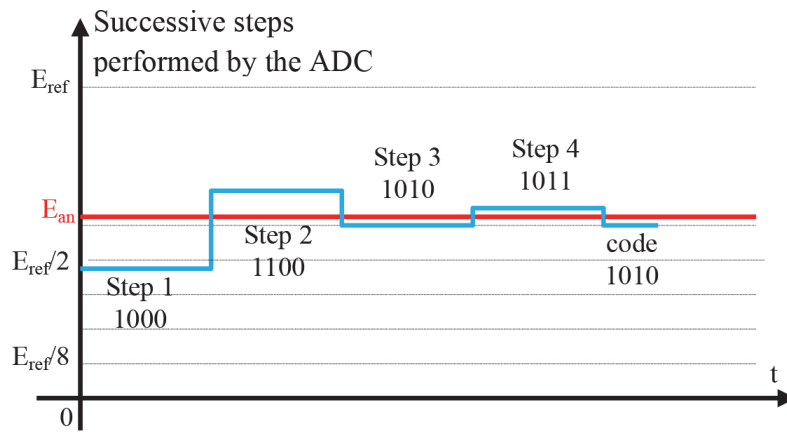




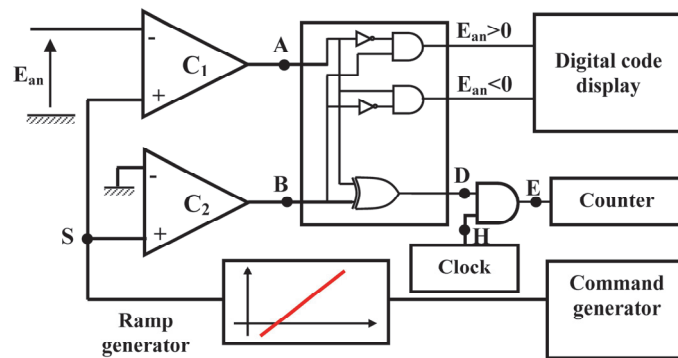
**Figure 2.17.** (a) Analog signal  $s(t)$  to be processed. (b) Corresponding sampled signal. (c) Each signal has its own frequency spectrum



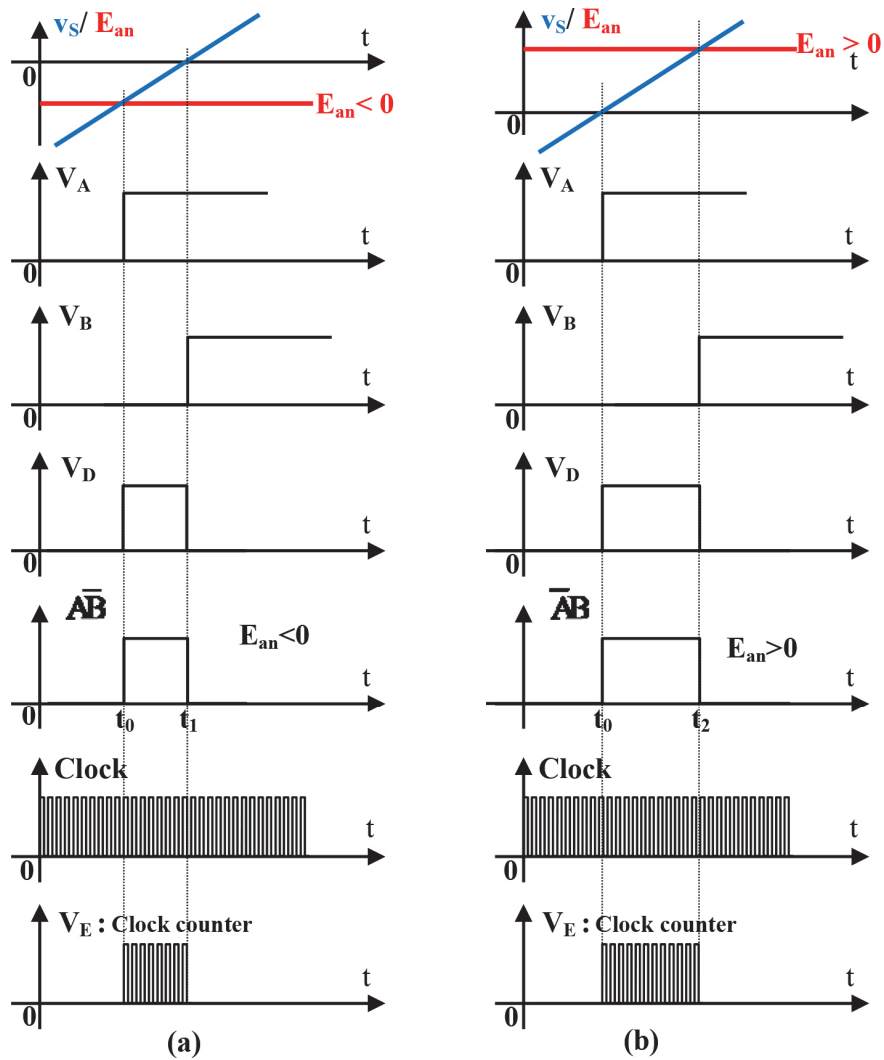
**Figure 2.27.** Quantification operation



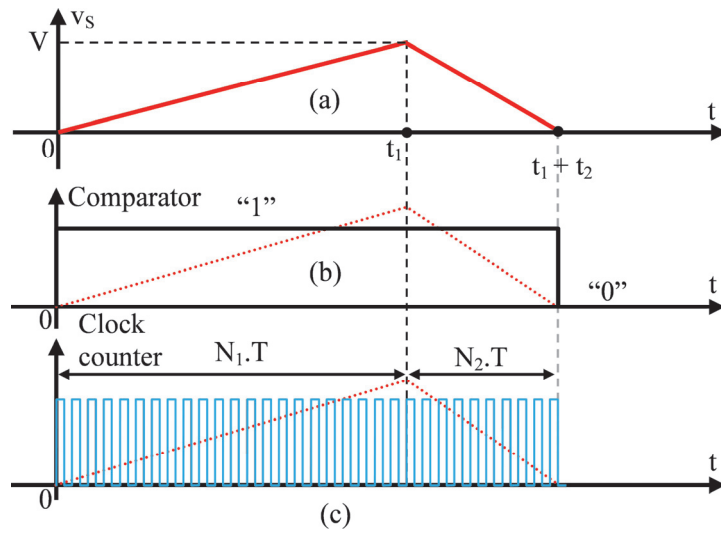
**Figure 2.34.** Various steps to obtain the code for an analog sample for a successive approximation ADC



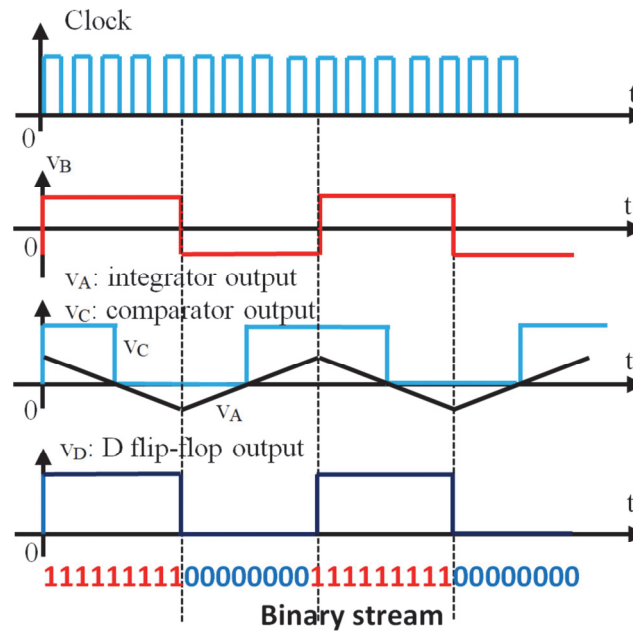
**Figure 2.36.** Schematic diagram of a single-ramp converter



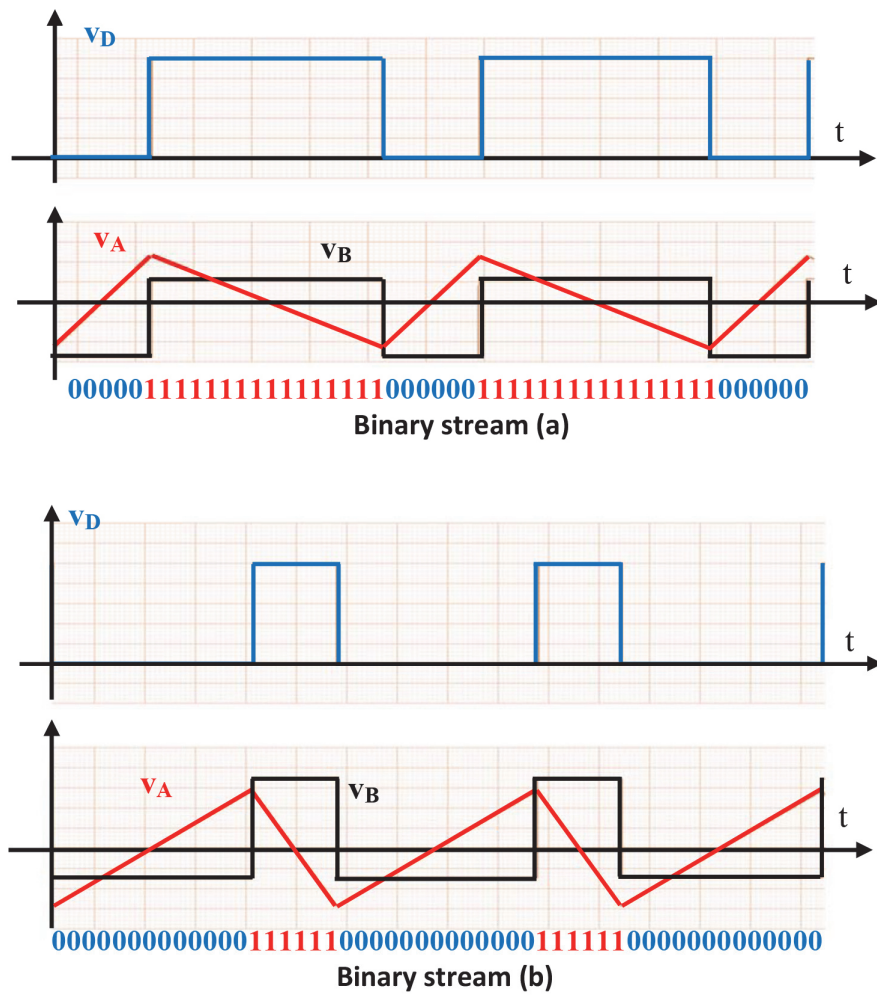
**Figure 2.38.** (a) Signals involved during conversion of a negative sample, (b) signals involved during conversion of a positive sample



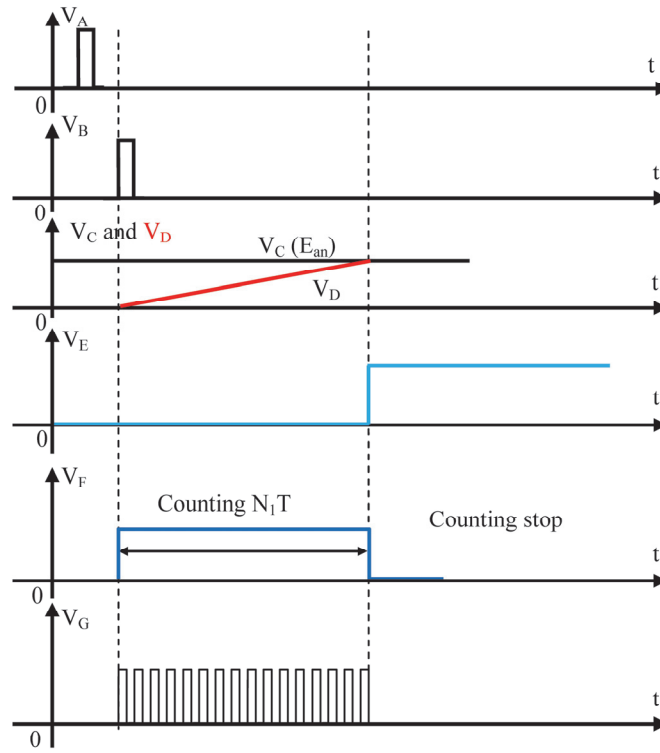
**Figure 2.43.** Different signals at the dual-slope ADC level



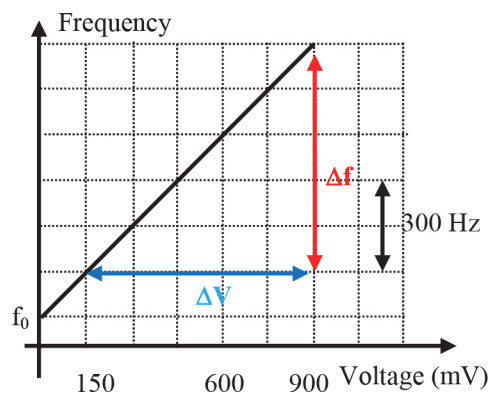
**Figure 2.46.** Signal representation at the level of the sigma-delta modulator with  $E_{an} = 0$



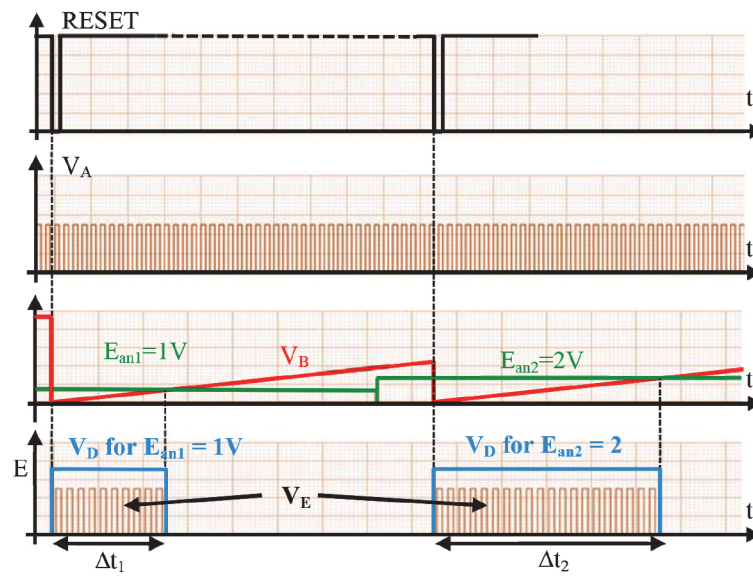
**Figure 2.47.** Signals identified in a sigma-delta ADC and binary output stream when (a) the sample  $E_{an} > 0$  and (b) the sample  $E_{an} < 0$



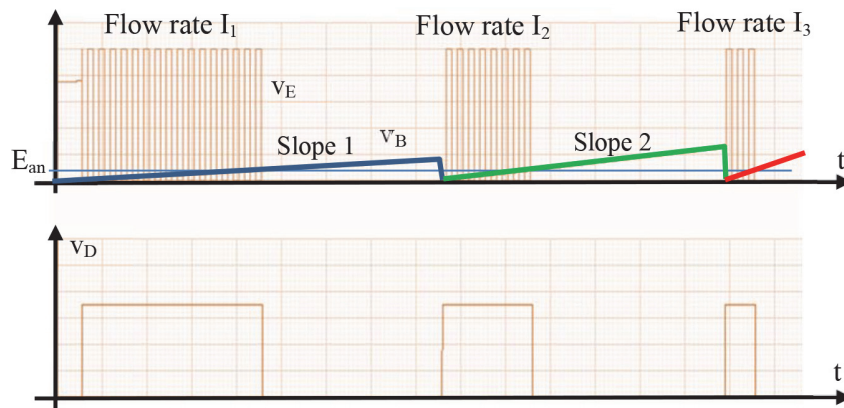
**Figure E8.2.** Signals involved at different points of the circuit presented in Figure E8.1



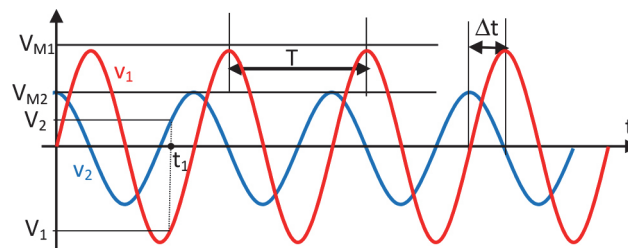
**Figure E9.5.** Slope of the VCO transfer curve



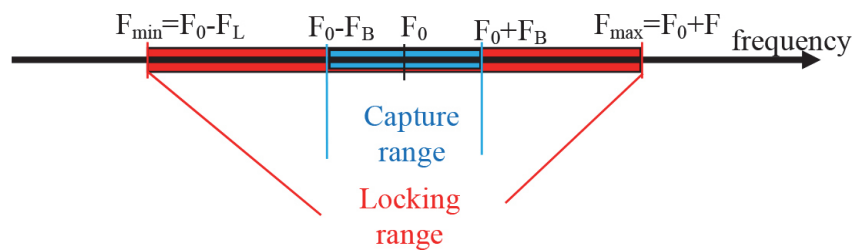
**Figure E11.2.** Evolution of various signals in the ADC under study



**Figure E11.3.** ADC accuracy in relation to the flow rate of the constant current generator with  $I_1 < I_2 < I_3$



**Figure 3.2.** Phase shift between two signals



**Figure 3.12.** Capture range and locking range



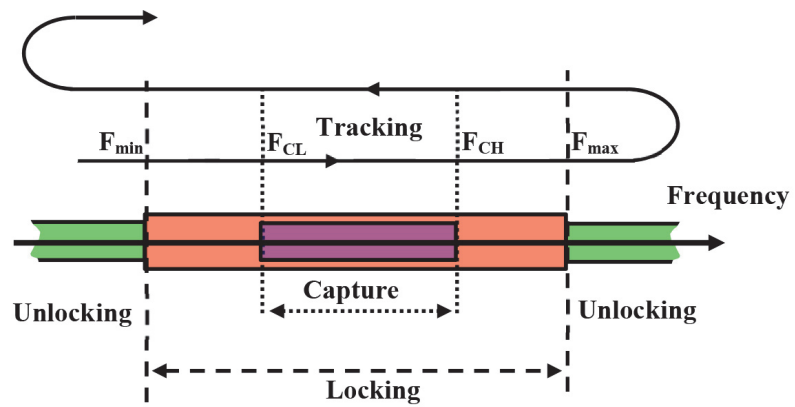


Figure 3.13. Operating mode of a PLL

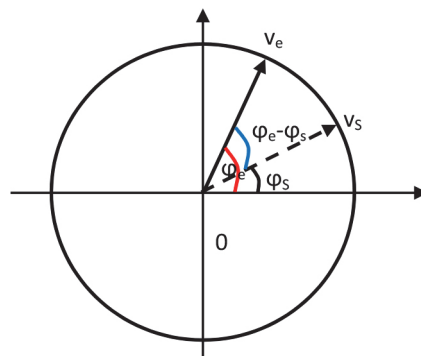
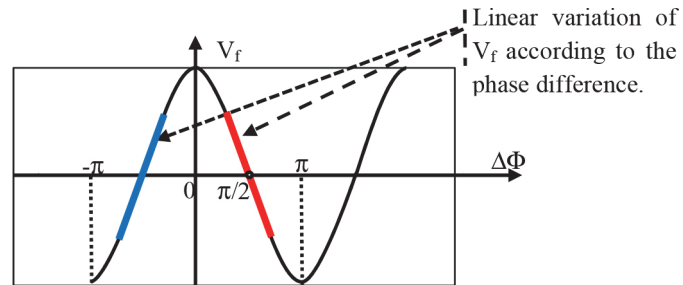
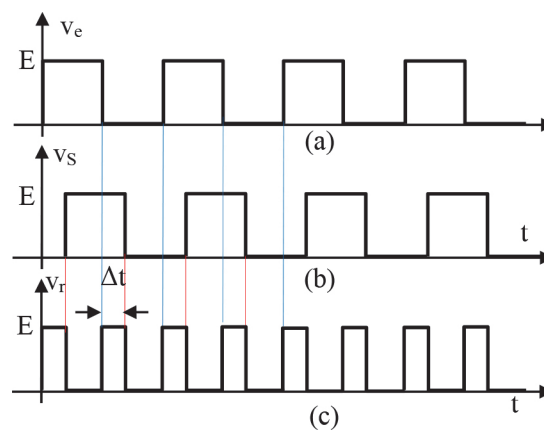


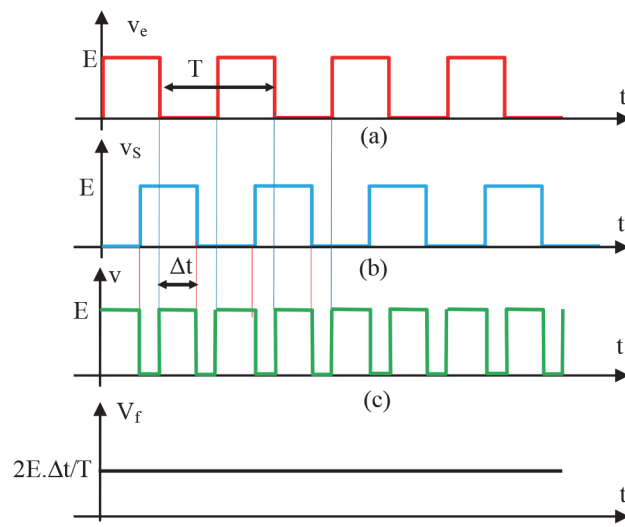
Figure 3.14. Vector representation of input and output signals



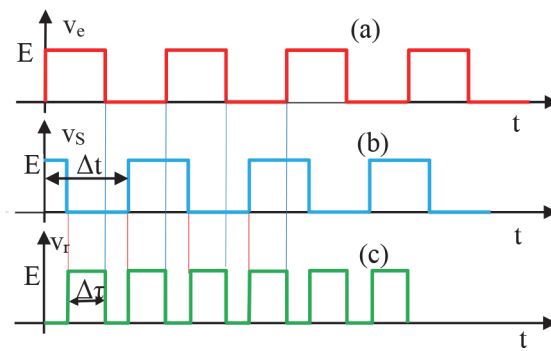
**Figure 3.16.** Evolution of the voltage  $V_f$  at the low-pass filter output based on the difference of phase shift  $\Delta\Phi$ . The variation is sinusoidal



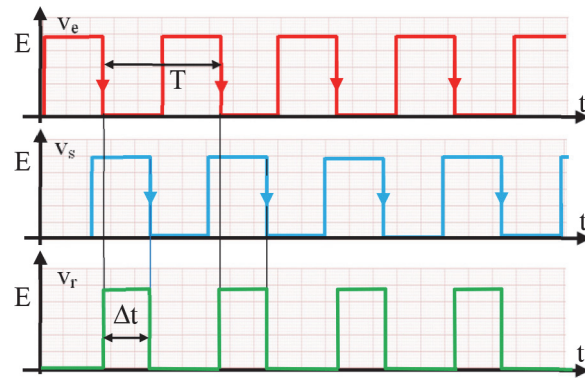
**Figure 3.18.** Various existing signals in a digital PLL. (a) reference signal  $v_e$ ; (b) signal  $v_s$  that can be found at the VCO output. (c) signal  $v_r$  that is found at the phase comparator output



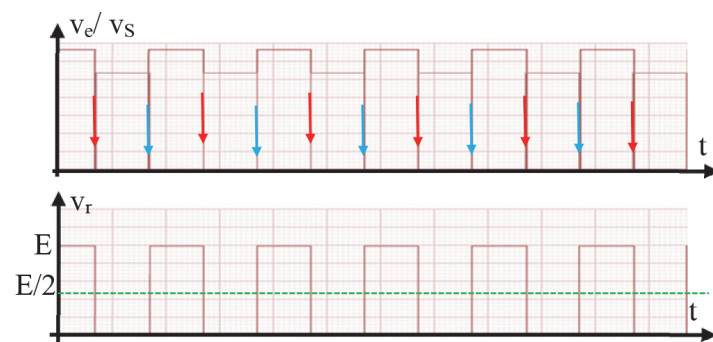
**Figure 3.19.** Different existing signals at the phase comparator input and output and the output of the low-pass filter ( $0 < \Delta\Phi < \pi$ )



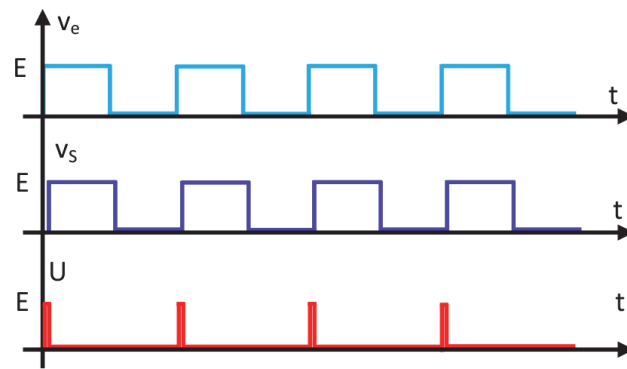
**Figure 3.20.** Signals at the phase comparator input and output when the phase shift is greater than  $\pi$



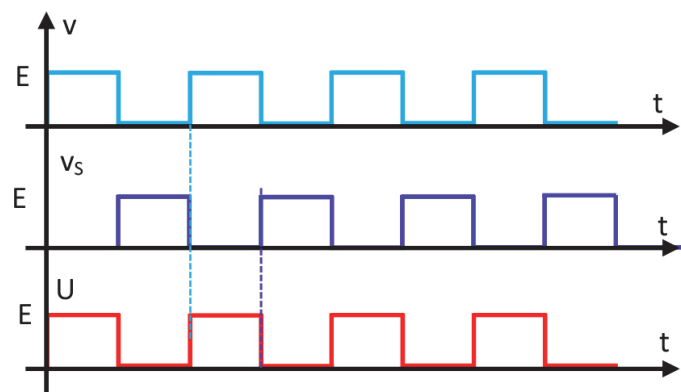
**Figure 3.23.** Evolution of signals at the RS flip-flop input and output of the phase comparator



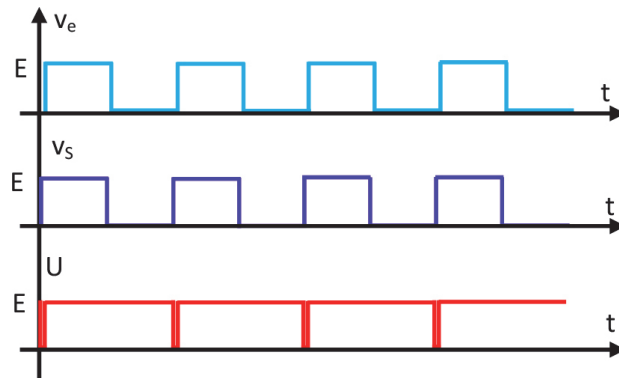
**Figure 3.25.** Phase comparator input and output signals



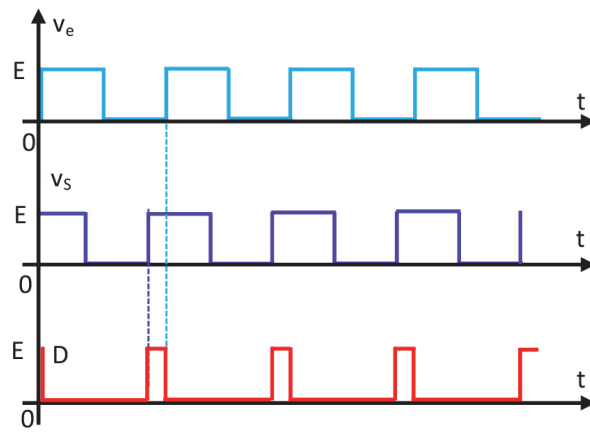
**Figure 3.28a.** Near-zero phase shift between  $v_e$  and  $v_s$



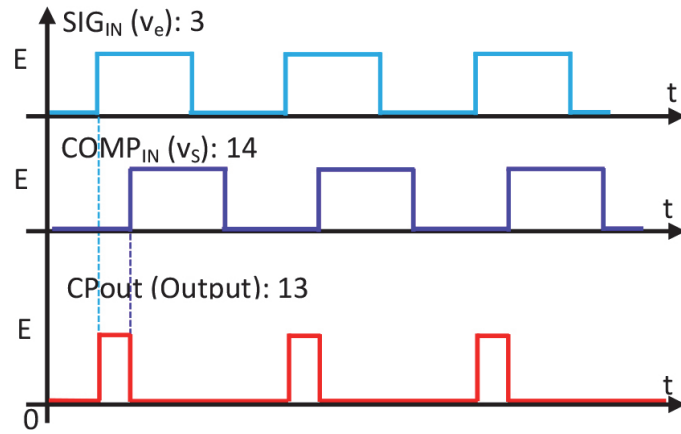
**Figure 3.28b.** Phase shift close to  $\pi$  between  $v_e$  and  $v_s$



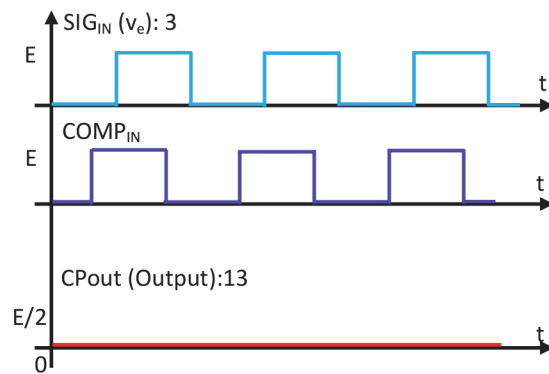
**Figure 3.28c.** Phase shift close to  $2\pi$  between  $v_e$  and  $v_s$



**Figure 3.29.** Signal  $v_e(t)$  is lagging compared to signal  $v_s(t)$ . Signal  $D$  (Down) is active



**Figure 3.35.** Input and output signals of the type-2 phase comparator of the 4046 IC (signal  $v_e$  is in leading phase compared to signal  $v_s$ )



**Figure 3.36.** Input and output signals of the type-2 phase comparator of the 4046 IC (signal  $v_e$  is in lagging phase compared to signal  $v_s$ )

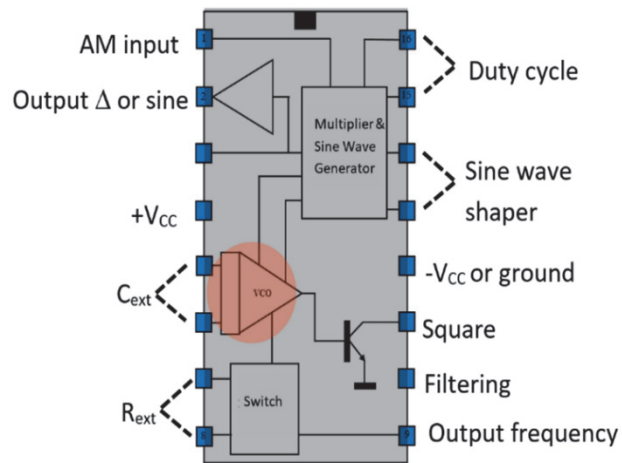


Figure 3.51. Internal diagram of the XR 2206 circuit

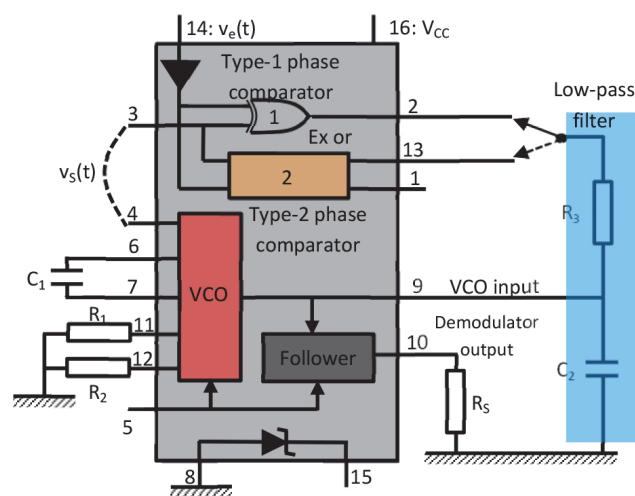
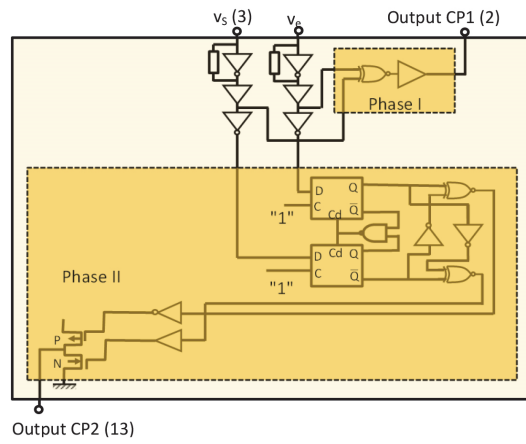
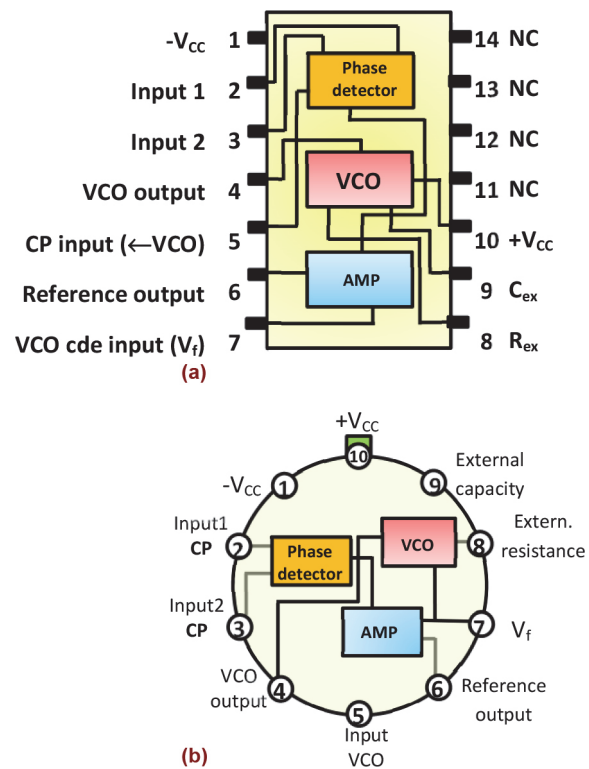


Figure 3.60. The 4046 IC and its block diagram

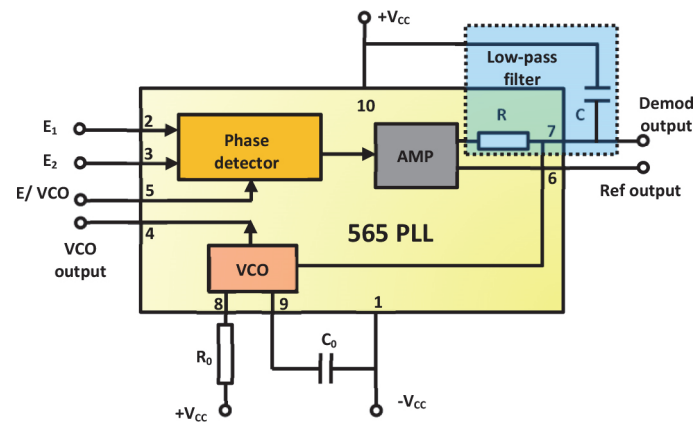




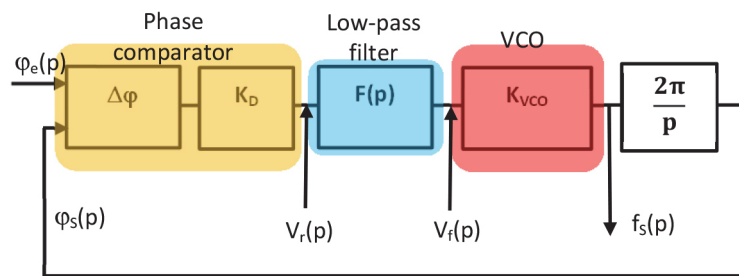
**Figure 3.63.** Schematic diagram of the two types of 4046 phase comparators



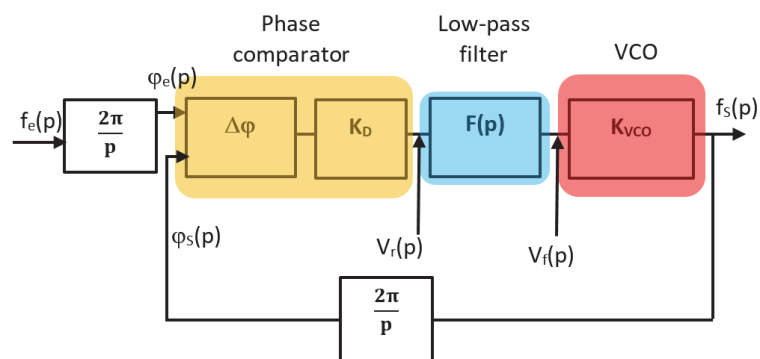
**Figure 3.64.** 565 PLL circuit in 14-pin DIL casing (a) and in 10-pin cylindrical-shape metal case (b)



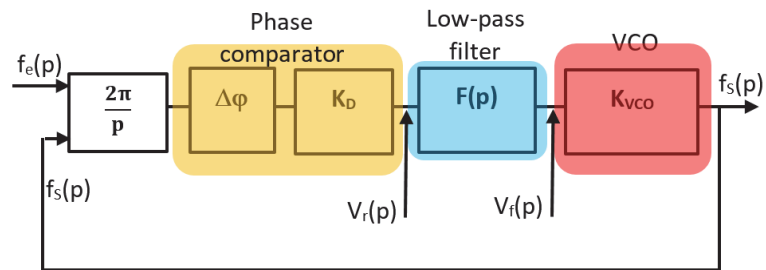
**Figure 3.65.** Block diagram of the 565 integrated PLL



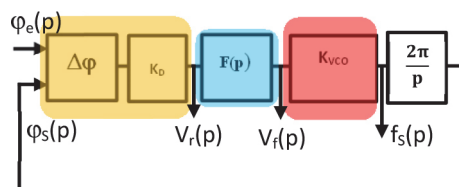
**Figure 3.68.** Block diagram of a PLL in terms of phase



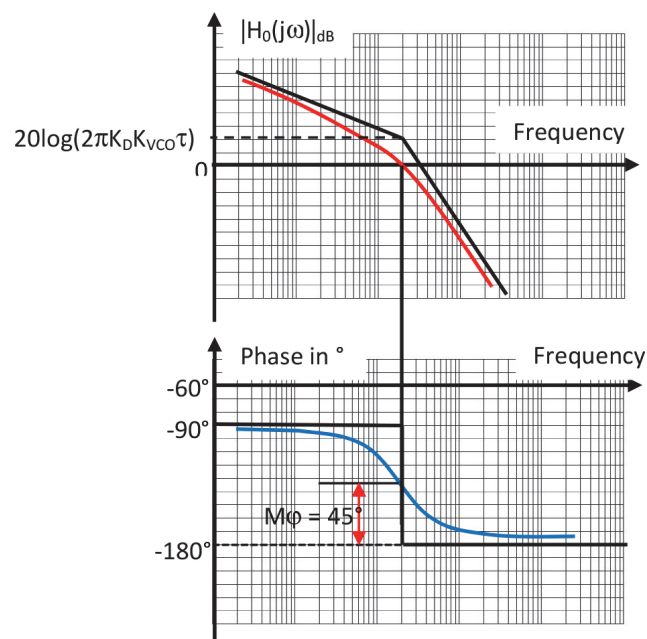
**Figure 3.69.** PLL block diagram; the input and output quantities are frequencies



**Figure 3.70.** PLL block diagram in terms of frequency with unity feedback



**Figure 3.71.** Diagram for the determination of the transfer function



**Figure 3.73.** Bode plot of the open-loop transfer function of the PLL with a first-order low-pass RC-type loop filter

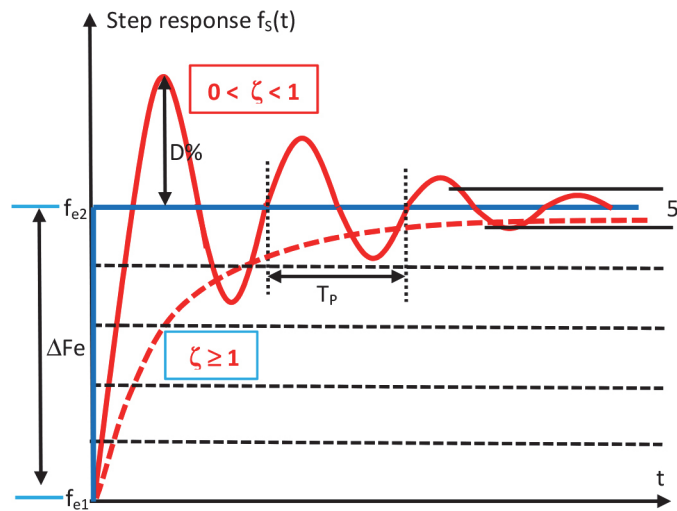


Figure 3.75. Second-order system step response

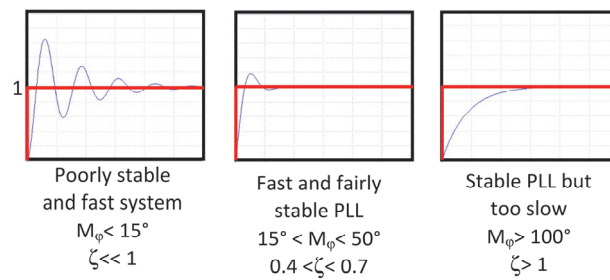


Figure 3.77. Evolution of a PLL step response according to the phase margin  $M_\phi$  and the damping coefficient

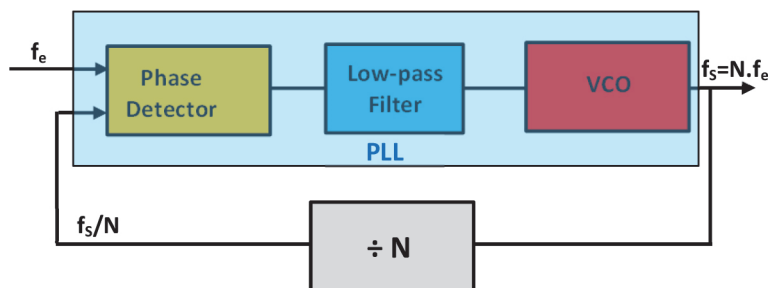


Figure 3.78. Principle of PLL-based frequency multiplying

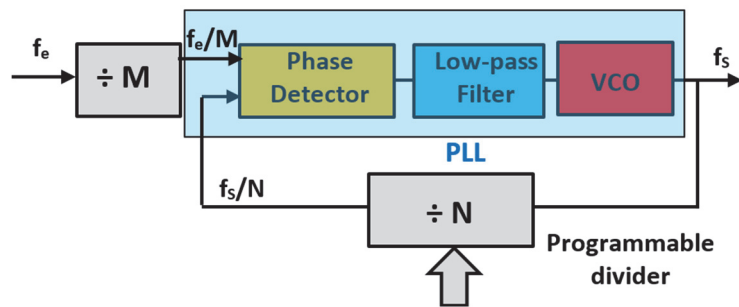


Figure 3.80. Principle of frequency synthesis using a PLL

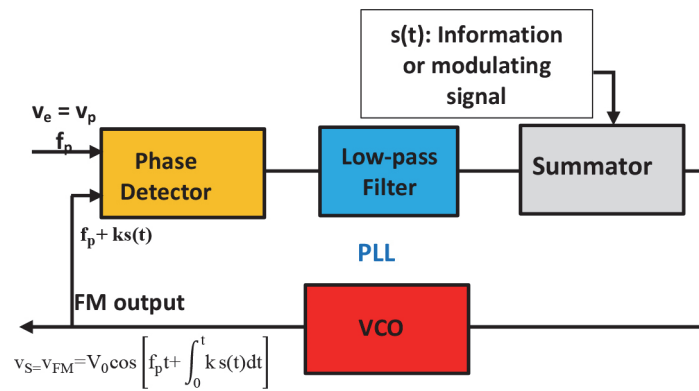


Figure 3.81. Frequency modulation using a PLL circuit

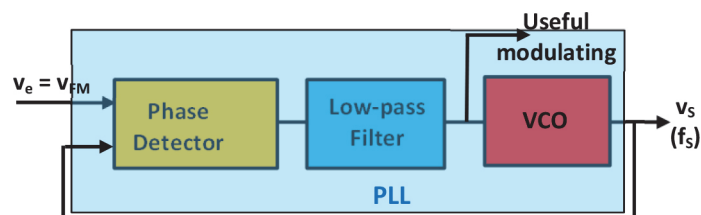
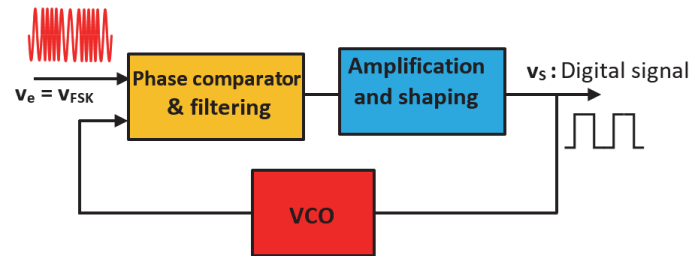
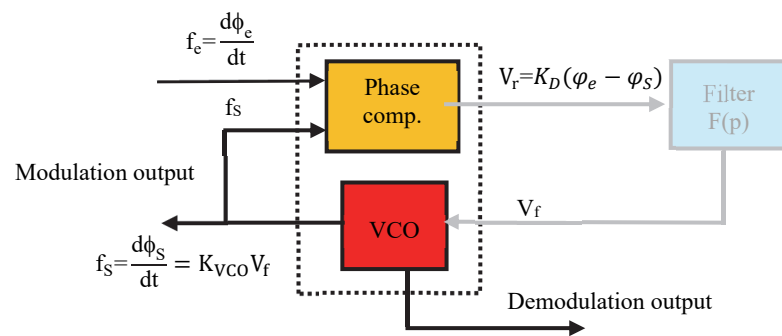


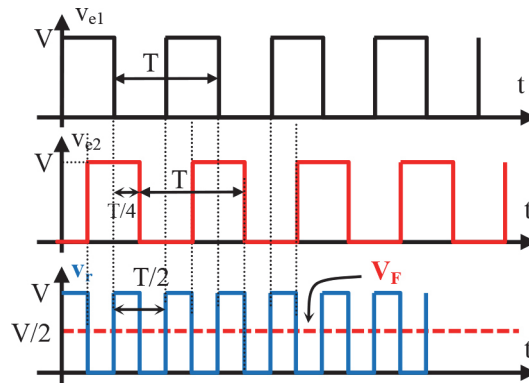
Figure 3.82. Frequency demodulation principle



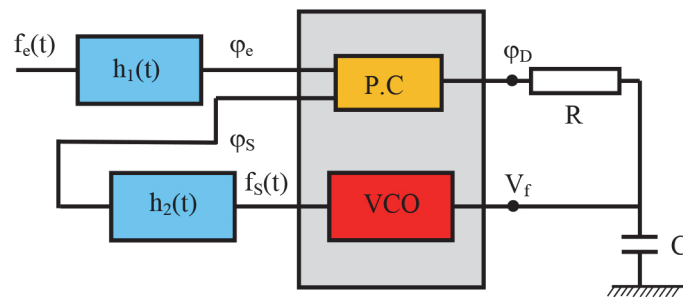
**Figure 3.84.** FSK demodulation principle



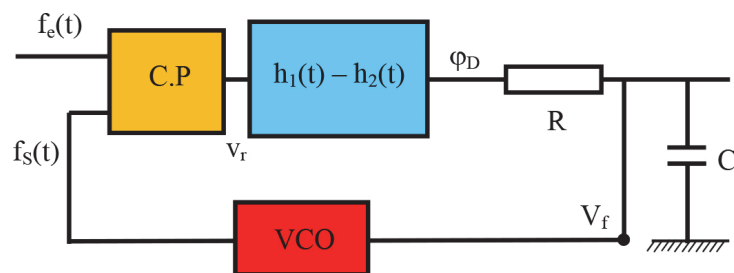
**Figure 3.85.** 4046 IC-based FSK modulation and demodulation



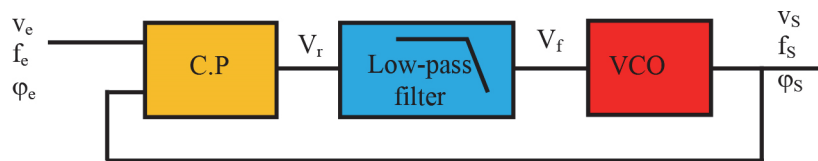
**Figure E3.2.** Representation of signals  $v_{e1}$ ,  $v_{e2}$ ,  $v_r$  and  $V_F$



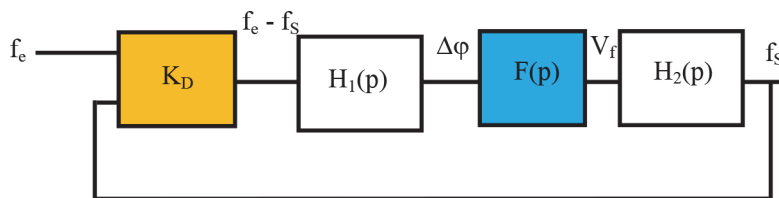
**Figure E8.3.** Block diagram under study



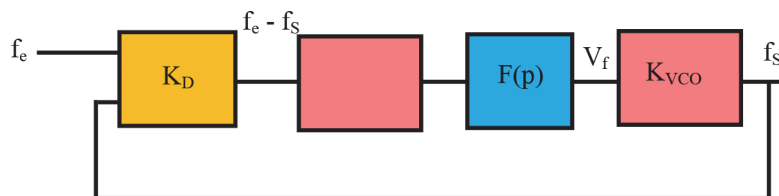
**Figure E8.4.** Simplified diagram of the PLL



**Figure E9.1.** PLL circuit

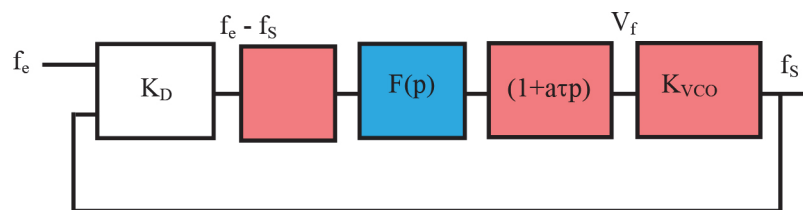


**Figure E9.2.** PLL block diagram

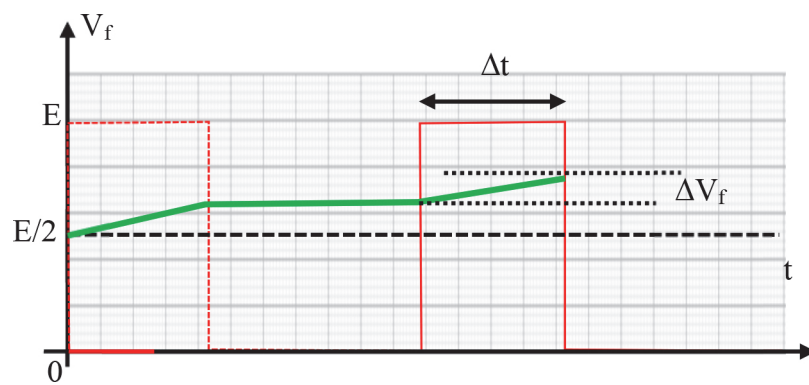


**Figure E9.5.** PLL block diagram with the definition of each block





**Figure E9.7.** PLL block diagram with the low-pass filter of Figure E9.4



**Figure E10.3.** Evolution of voltage  $V_f$  at the capacitor terminals