
Contents

Preface	ix
Chapter 1. Introduction of Real-time Image Processing	1
1.1. General image processing presentation	1
1.2. Real-time image processing	5
Chapter 2. Hardware Architectures for Real-time Processing	13
2.1. History of image processing hardware platforms	13
2.2. General-purpose processors	14
2.3. Digital signal processors	15
2.4. Graphics processing units	18
2.5. Field programmable gate arrays	19
2.6. SW/HW codesign of real-time image processing	21
2.7. Image processing development environment description ..	23
2.8. Comparison and discussion	26
Chapter 3. Rapid Prototyping of Parallel Reconfigurable Instruction Set Processor for Efficient Real-Time Image Processing	31
3.1. Context and problematic	32
3.2. Related works	34
3.3. Design exploration framework	36
3.4. Case study: RISP conception and synthesis for spatial transforms	40

3.4.1. Digital DCT algorithm implementations	40
3.4.2. Rapid prototyping of DCT RISP conception	42
3.4.3. RISP simulation and synthesis for 2D-DCT	45
3.5. Hardware implementation of spatial transforms on an FPGA-based platform	49
3.6. Discussion and conclusion	53
Chapter 4. Exploration of High-Level Synthesis Technique	55
4.1. Introduction of HLS technique	55
4.2. Vivado_HLS process presentation	60
4.2.1. Control and datapath extraction	61
4.2.2. Scheduling and binding	62
4.3. Case of HLS application: FPGA implementation of an improved skin lesion assessment method	65
4.3.1. KMGA method description	66
4.3.2. KMGA method optimization	71
4.3.3. HCR-KMGA implementation onto FPGA using HLS technique	82
4.3.4. Implementation evaluation experiments	85
4.4. Discussion	91
Chapter 5. CDMS4HLS: A Novel Source- To-Source Compilation Strategy for HLS-Based FPGA Design	93
5.1. S2S compiler-based HLS design framework	94
5.2. CDMS4HLS compilation process description	96
5.2.1. Function inline	97
5.2.2. Loop manipulation	98
5.2.3. Symbolic expression manipulation	99
5.2.4. Loop unwinding	101
5.2.5. Memory manipulation	102
5.3. CDMS4HLS compilation process evaluation	104
5.3.1. Performances improvement evaluation	104
5.3.2. Comparison experiment	108
5.4. Discussion	110
Chapter 6. Embedded Implementation of VHR Satellite Image Segmentation	113
6.1. LSM description	114
6.1.1. Background	114

6.1.2. Level set equation	116
6.1.3. LBM solver	119
6.2. Implementation and optimization presentation	120
6.2.1. Design flow description	120
6.2.2. Algorithm analysis	122
6.2.3. Function inline	124
6.2.4. Loop manipulation.	126
6.2.5. Symbol expression manipulation	128
6.2.6. Loop unwinding	129
6.3. Experiment evaluation	131
6.3.1. Parameter configuration.	131
6.3.2. Function verification	133
6.3.3. Optimization evaluation	135
6.3.4. Performance comparison.	137
6.4. Discussion and conclusion	138
Chapter 7. Real-time Image Processing with Very High-level Synthesis.	141
7.1. VHLS motivation	142
7.2. Image processing from Matlab to FPGA-RTL	143
7.3. VHLS process presentation	144
7.3.1. Dynamic variable	145
7.3.2. Operation polymorphism problem	146
7.3.3. Built-in function problem	147
7.4. VHLS implementation issues	147
7.4.1. Work flow.	148
7.4.2. Intermediate code versus RTL.	149
7.4.3. SSC versus HLS	149
7.4.4. Verification and evaluation	150
7.5. Future work for real-time image processing with VHLS.	150
Bibliography	153
Index	163